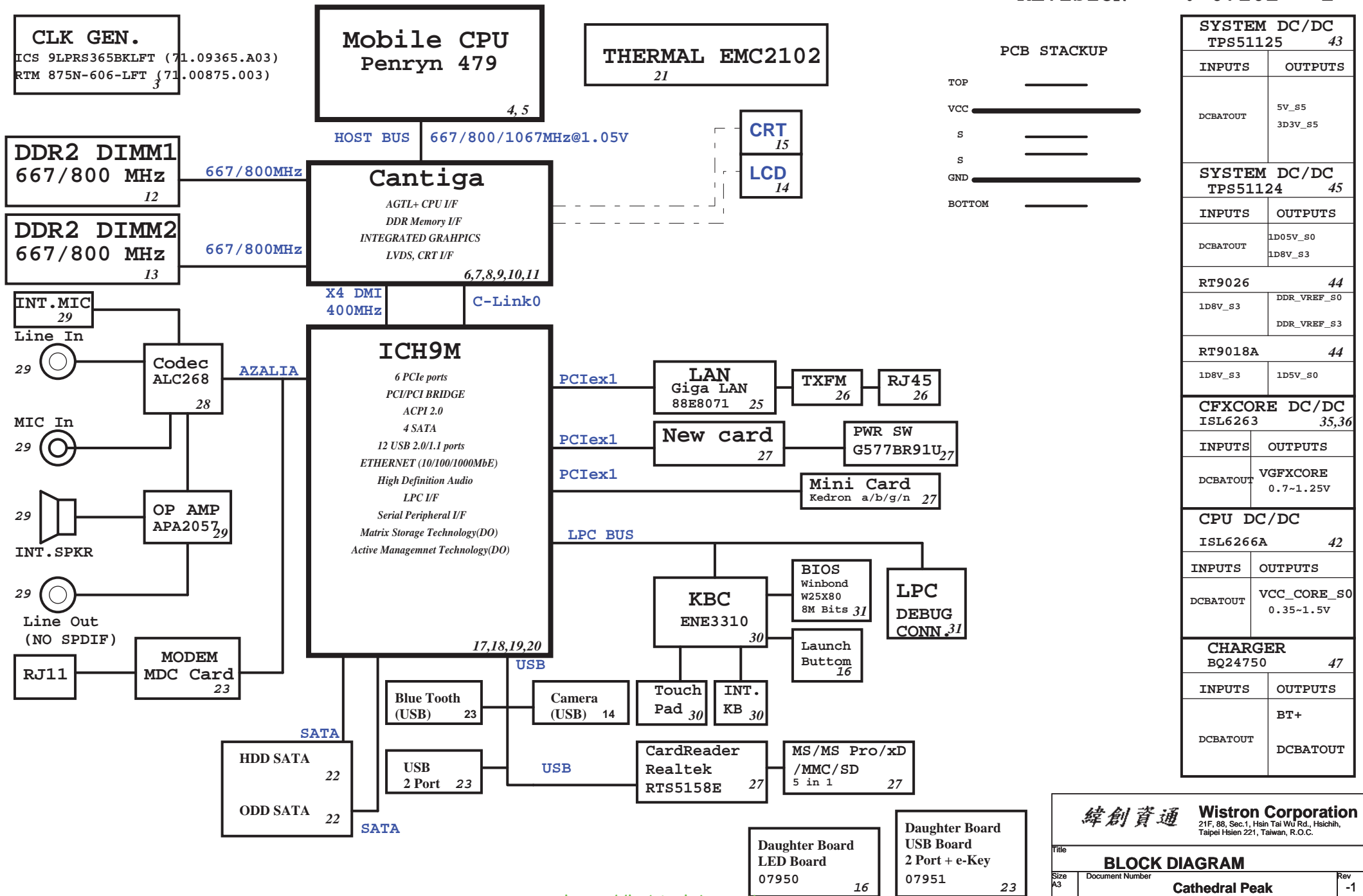


Project code: 91.4J501.001
PCB P/N : 48.4J501.001
REVISION : 07261 - 1



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

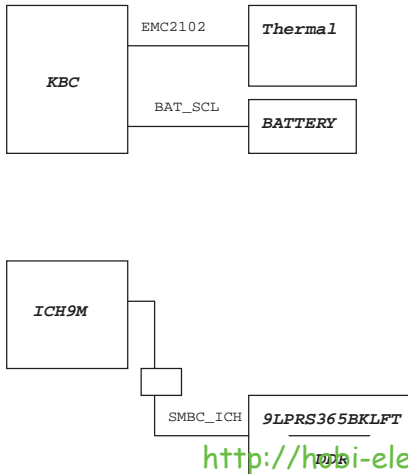
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	NC
4	USB3
5	Bluetooth
6	NC
7	MINIC1
8	WEBCAM
9	NEW1
10	Card Reader
11	NC

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSPLVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

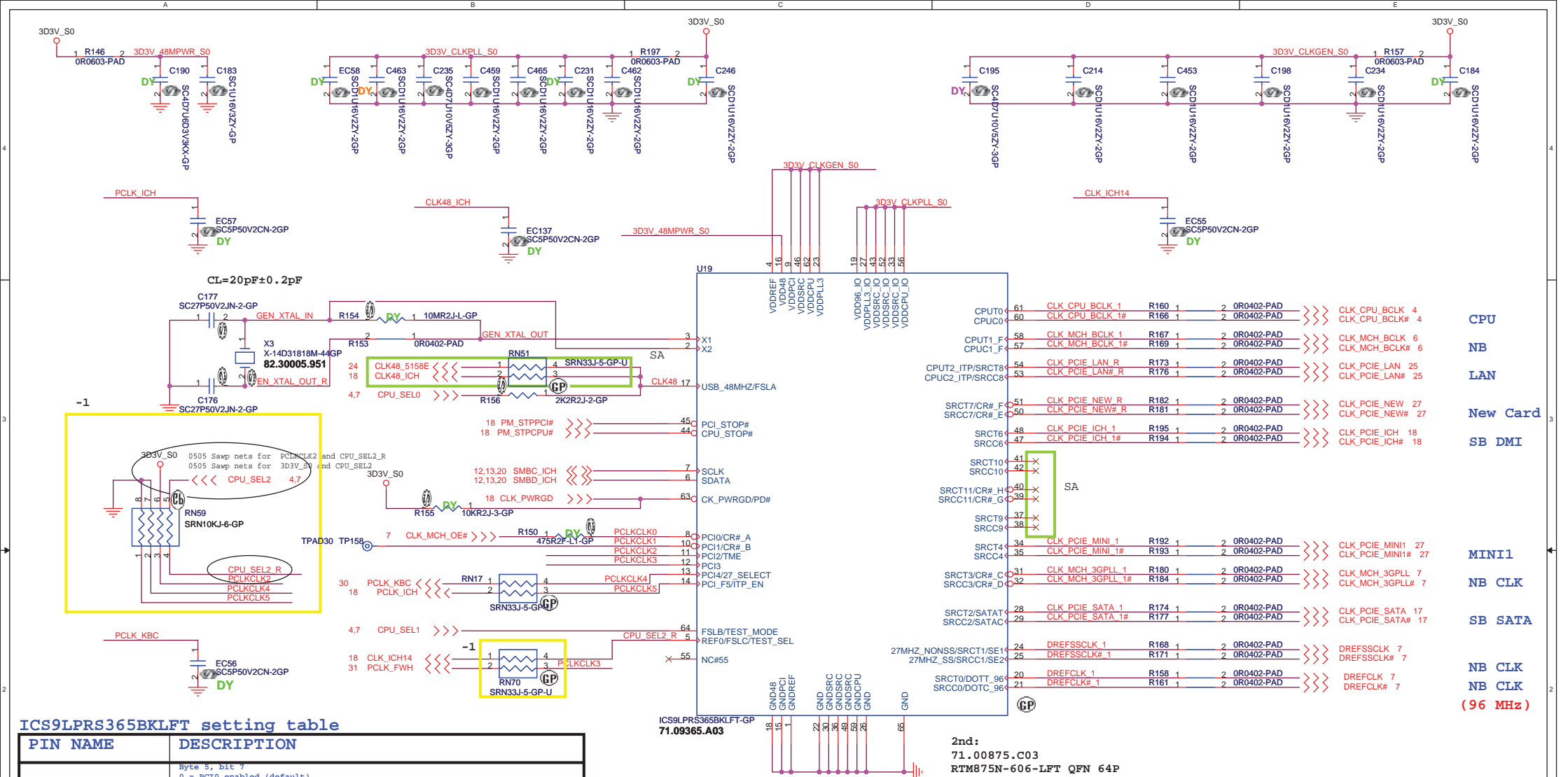
NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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Title		
Reference		
Size A3	Document Number	Rev -1
Date: Monday, May 05, 2008	Sheet 2 of 42	



CPU
NB
LAN
New Card
SB DMI
MINI1
NB CLK
SB SATA
NB CLK
NB CLK
(96 MHz)

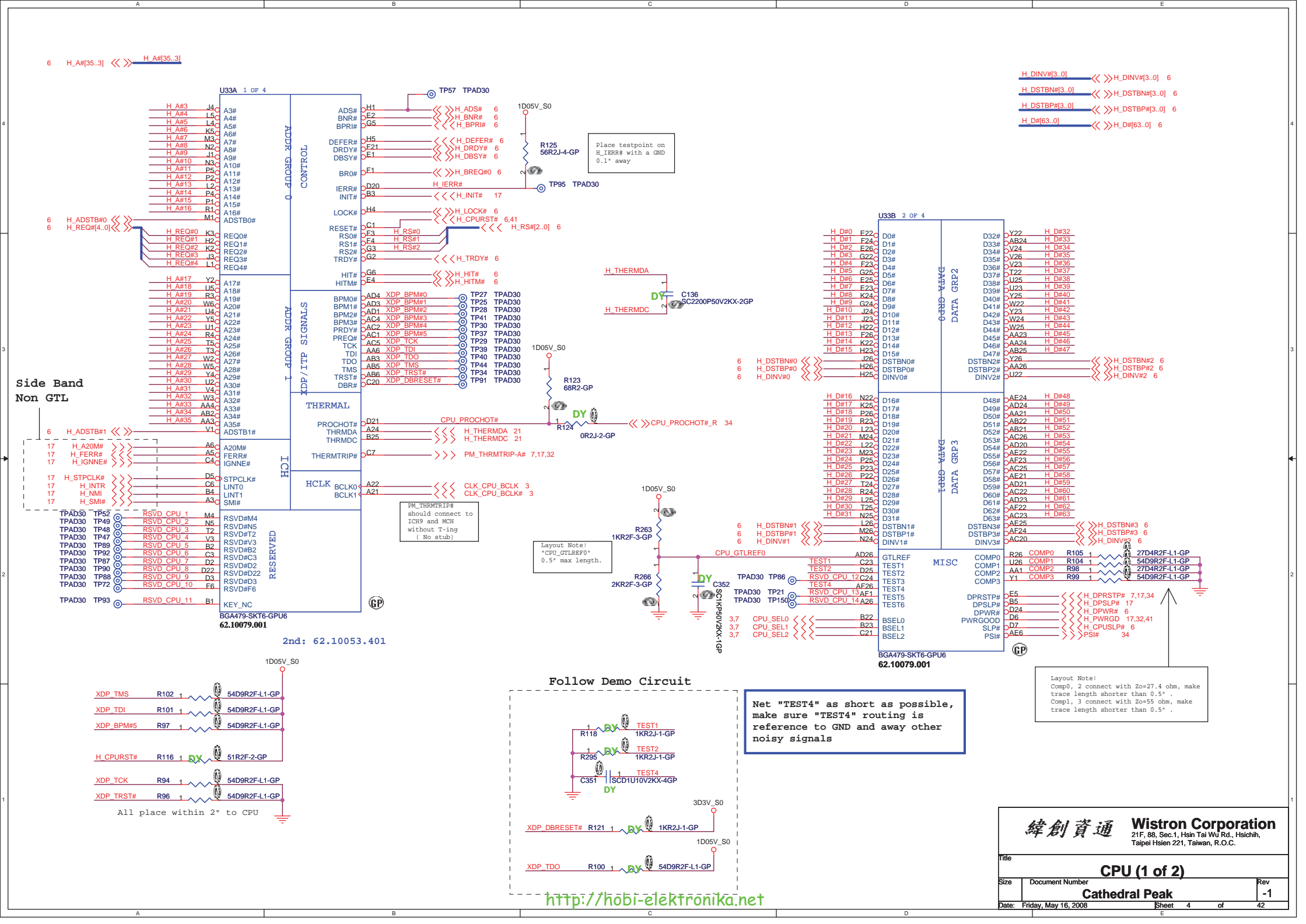
SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

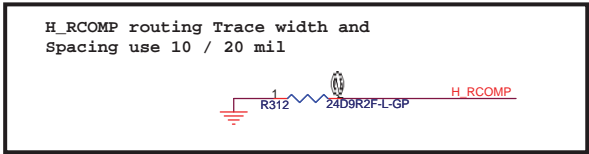
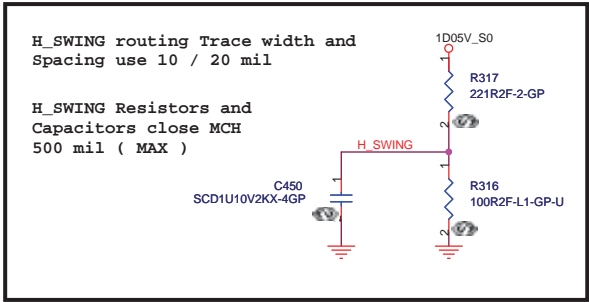
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Clock Generator

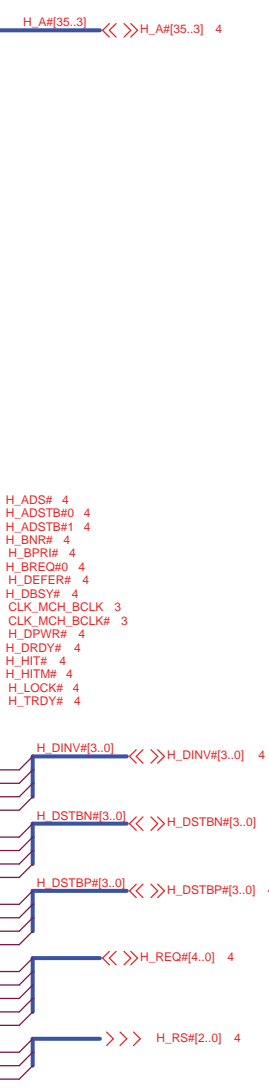
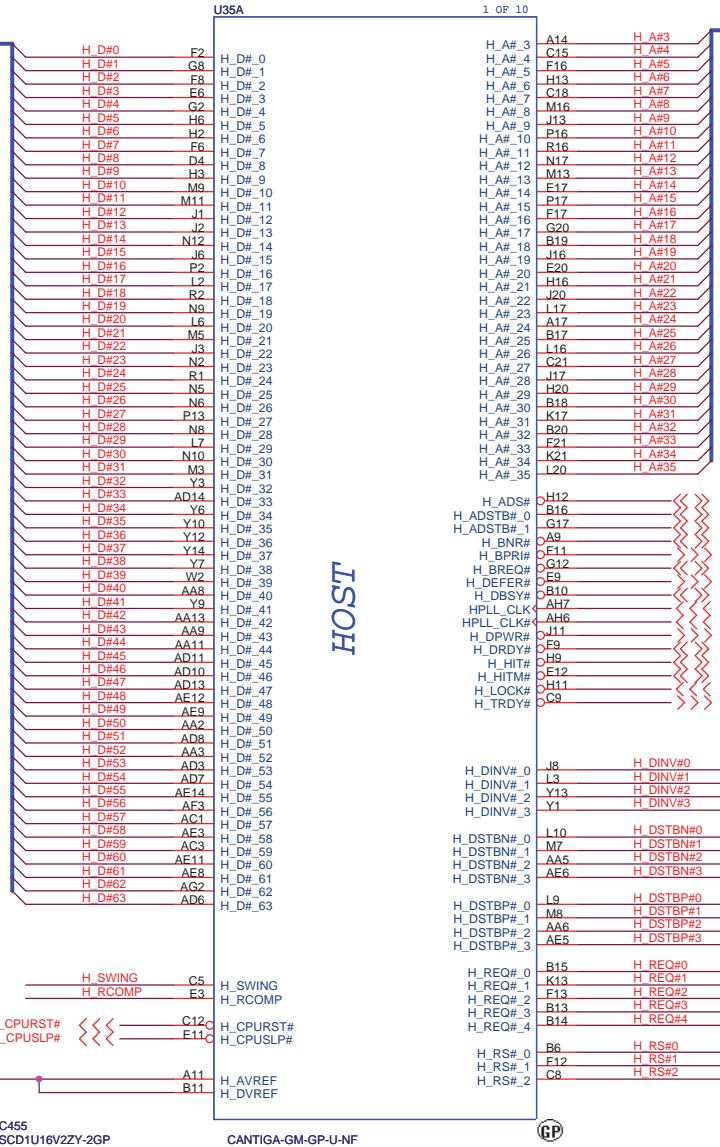
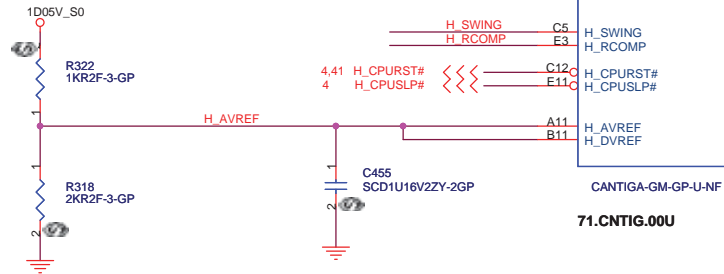
Size: Document Number: Cathedral Peak Rev: -1

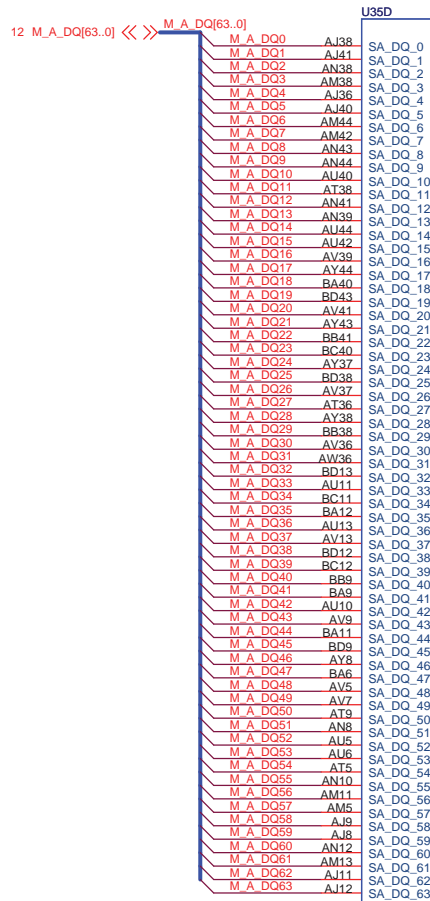
Date: Friday, May 16, 2008 Sheet: 3 of 42



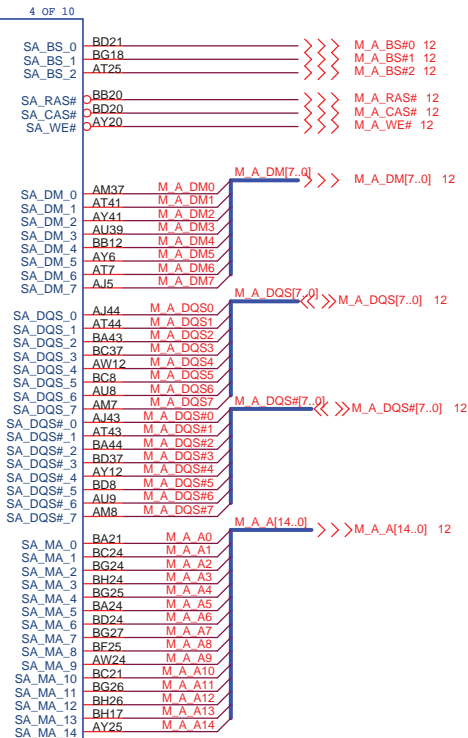


Place them near to the chip (< 0.5")



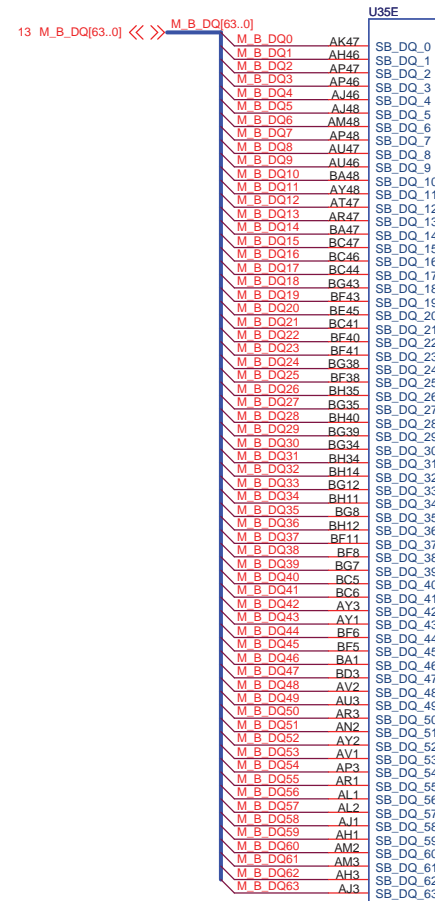


DDR SYSTEM MEMORY A

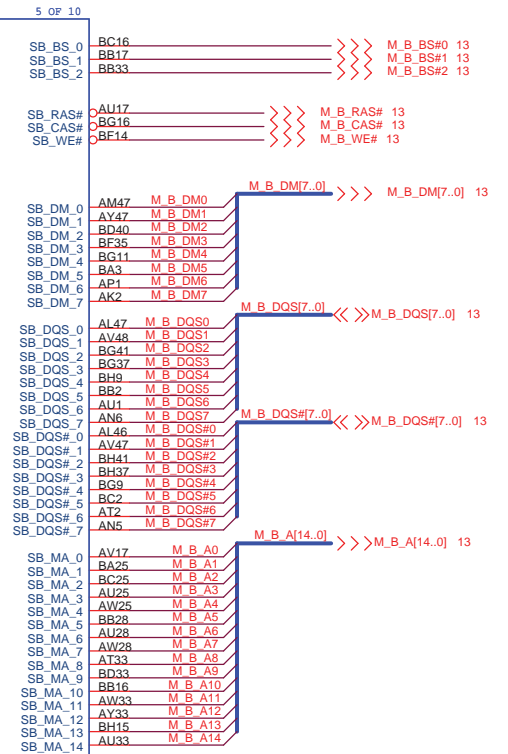


CANTIGA-GM-GP-U-NF

71.CNTIG.00U



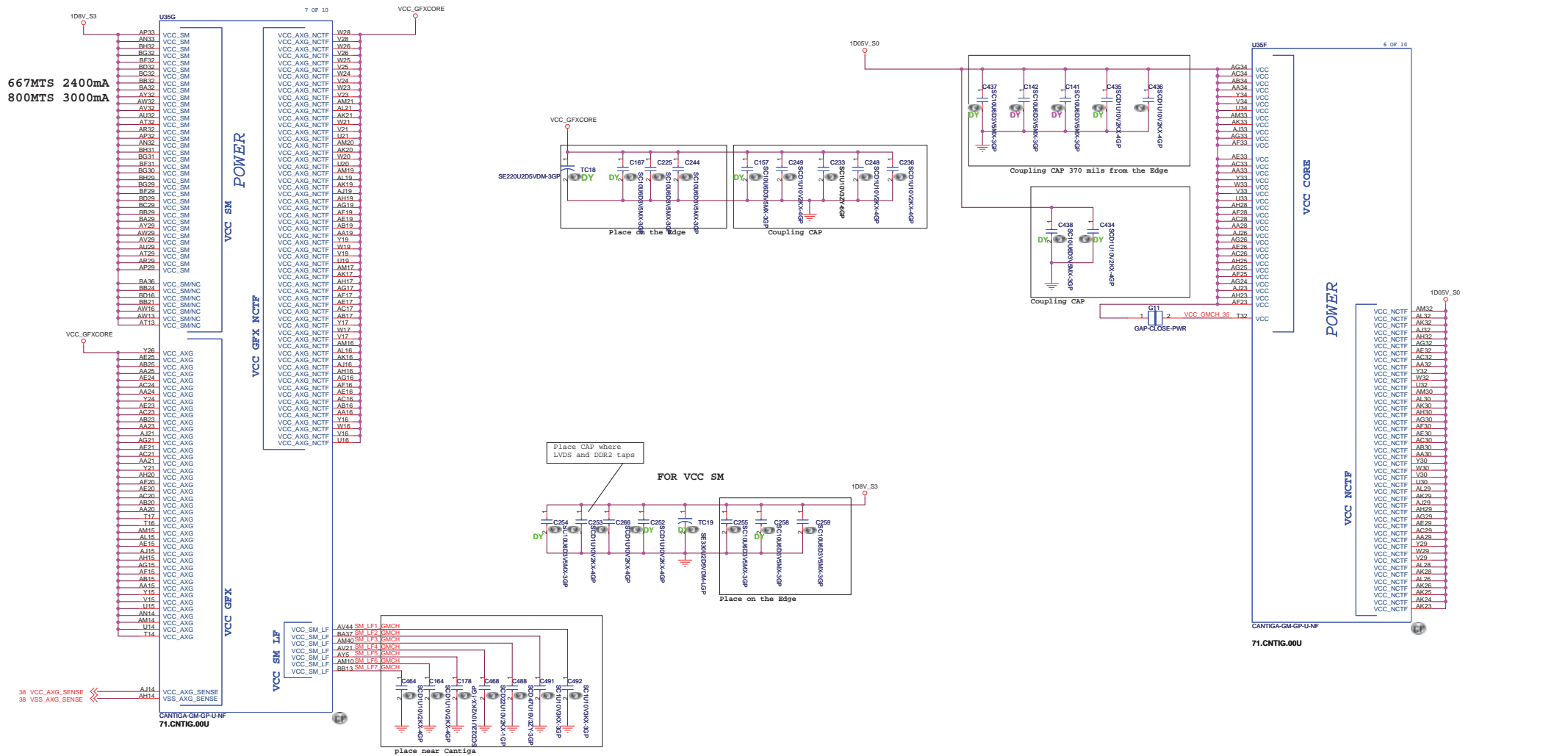
DDR SYSTEM MEMORY B

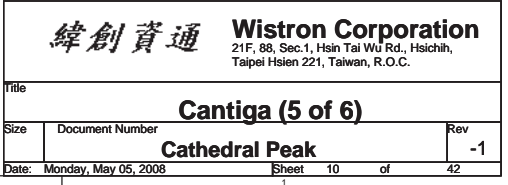


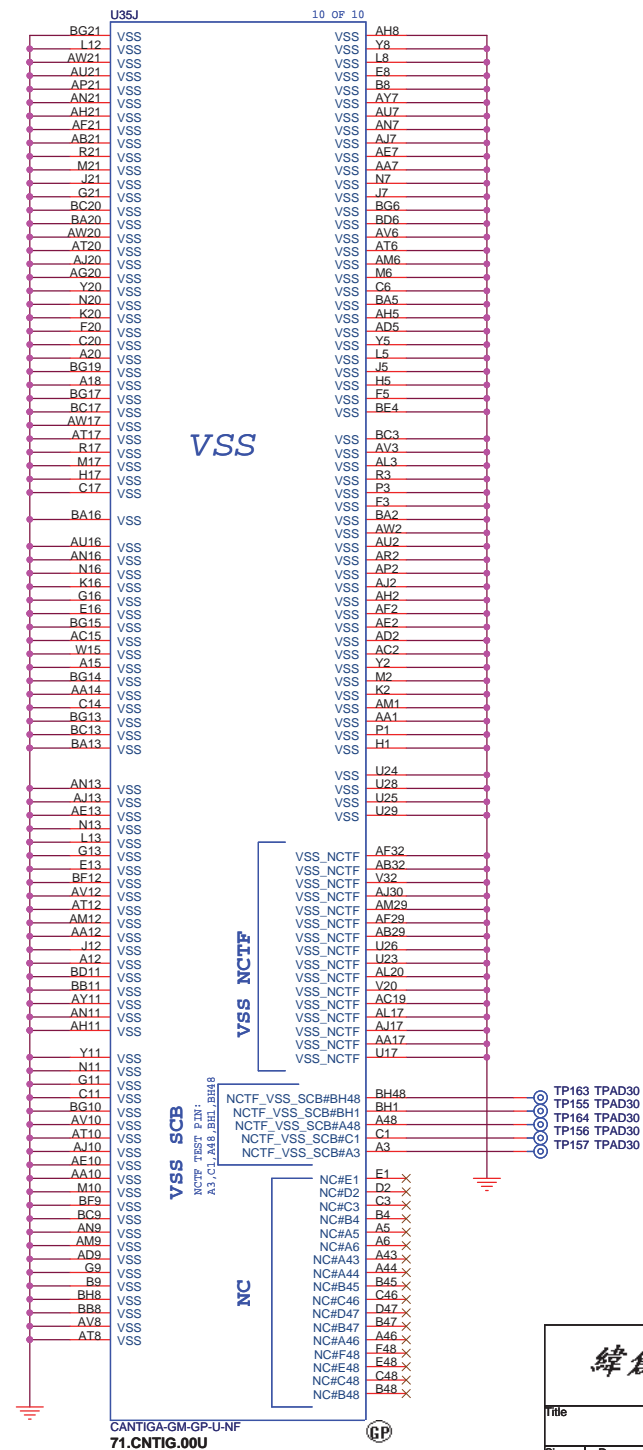
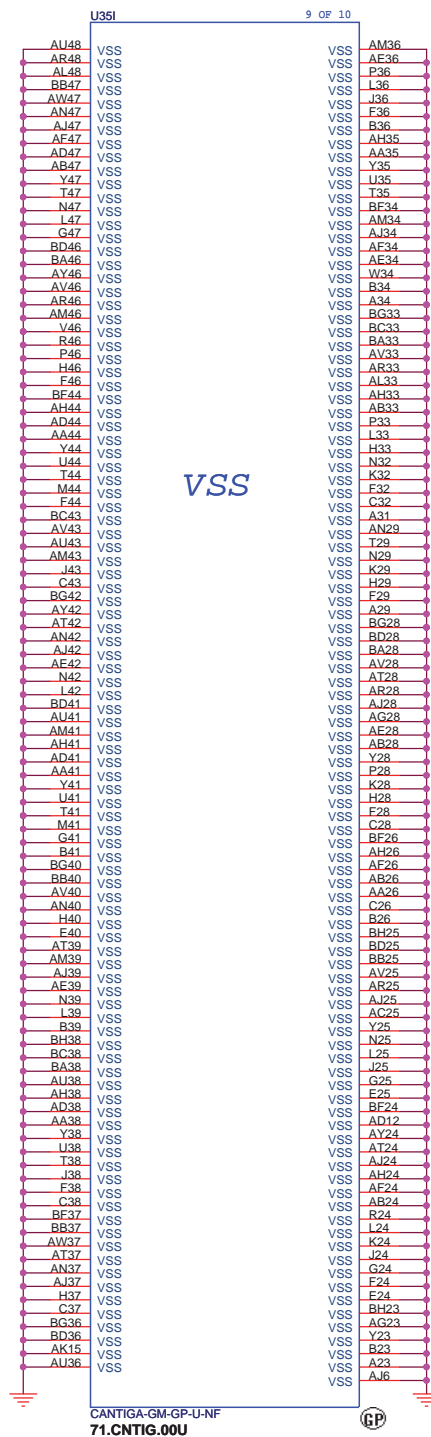
CANTIGA-GM-GP-U-NF

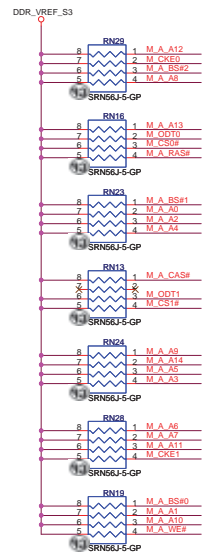
71.CNTIG.00U

667MTS 2400mA
800MTS 3000mA





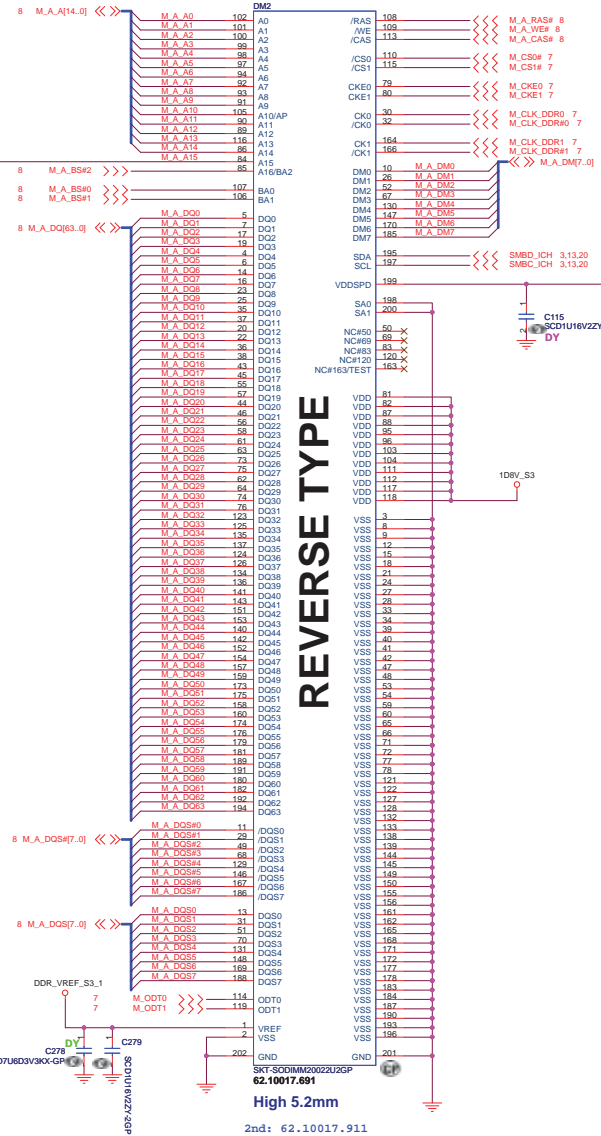
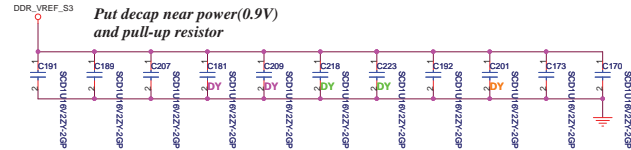




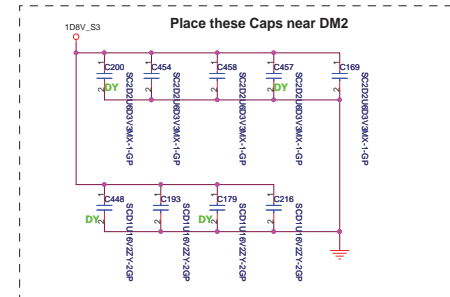
PARALLEL TERMINATION

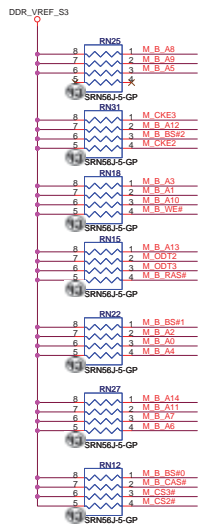
Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor



REVERSE TYPE



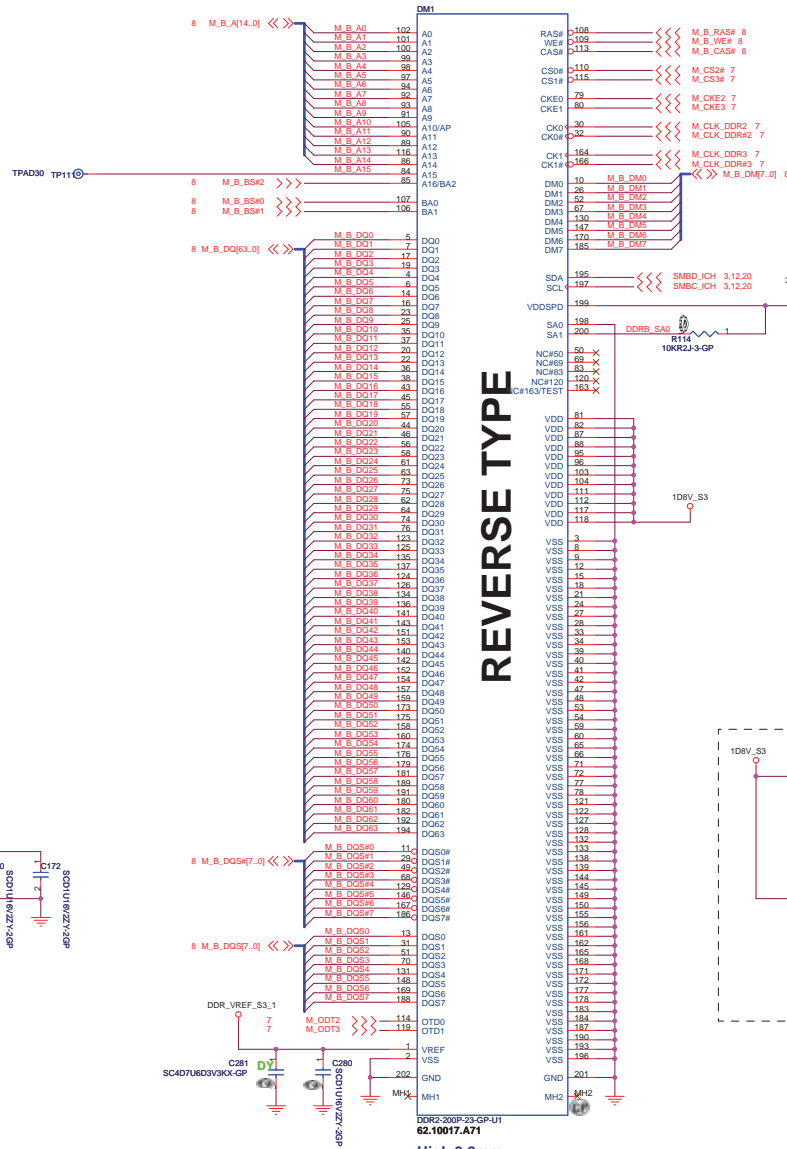
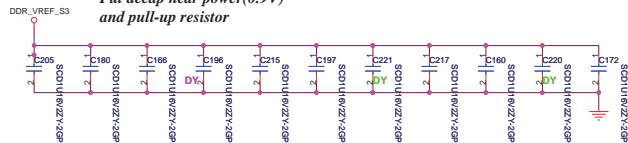


PARALLEL TERMINATION

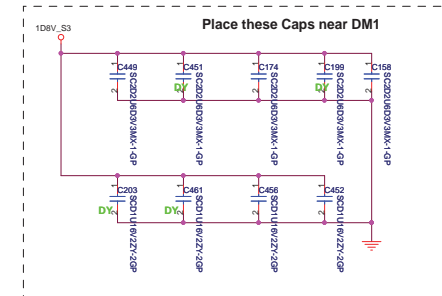
Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

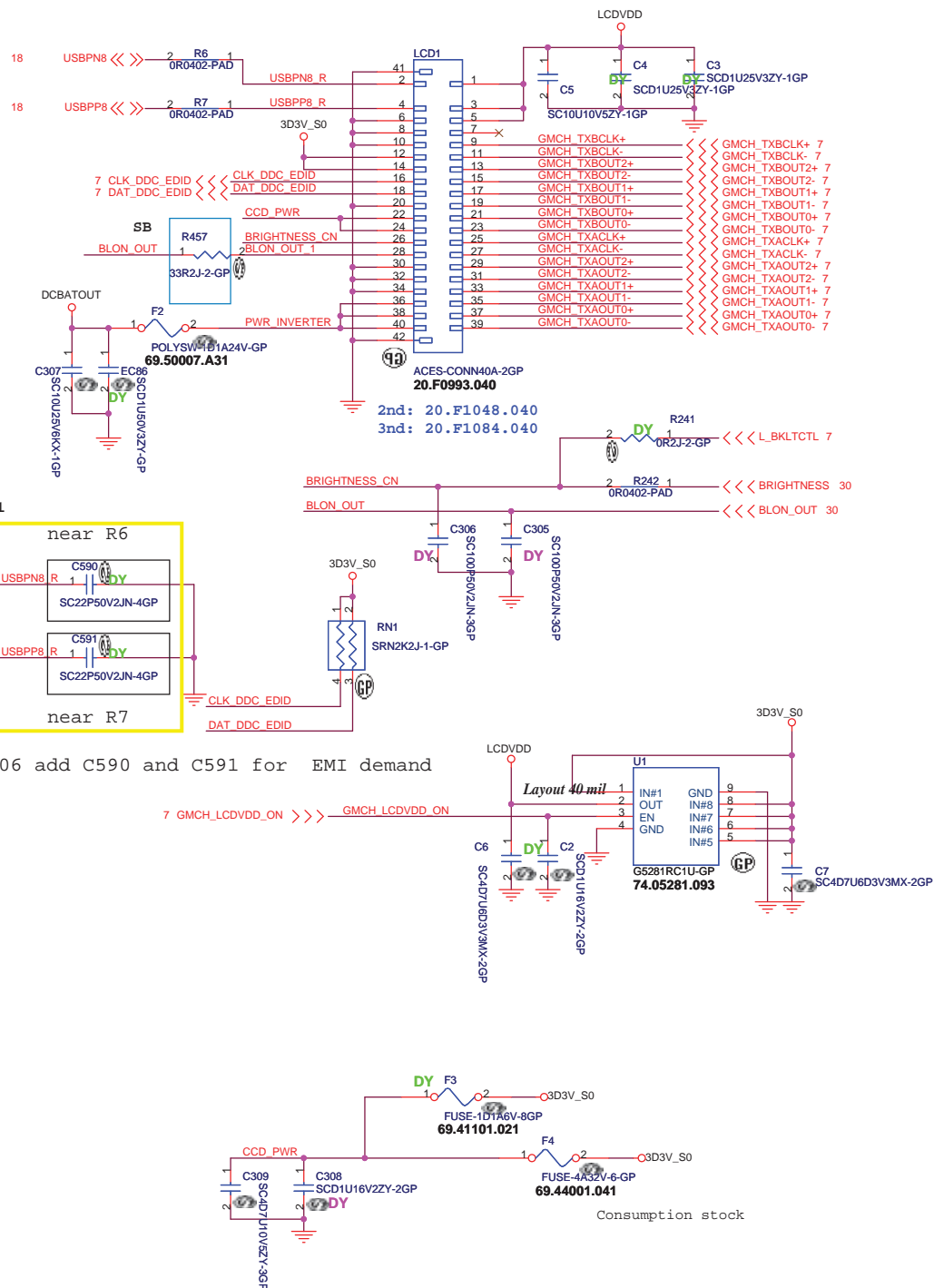
Put decap near power(0.9V) and pull-up resistor



2nd: 62.10017.B51



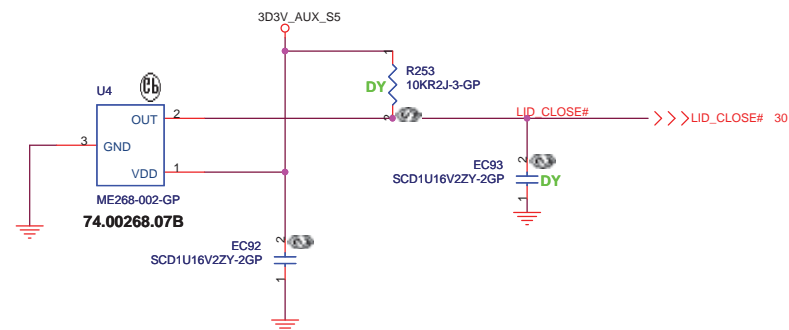
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWL
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch



74.00268.A7B

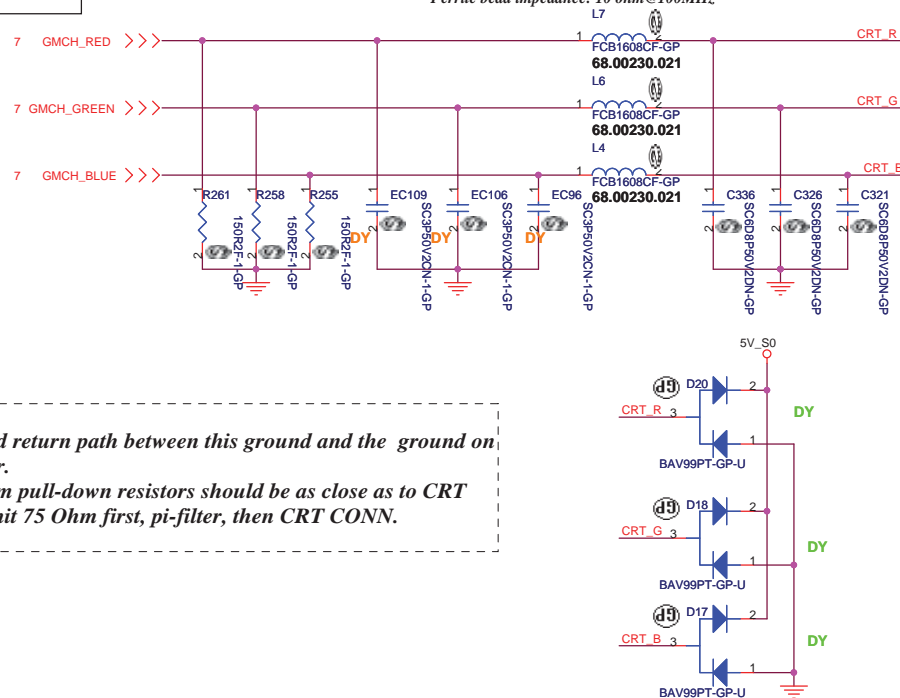
74.00268.C7B

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Title			
LCD CONN			
Size	Document Number		Rev
	Cathedral Peak		-1
Date:	Friday, May 16, 2008	Sheet	14 of 42

Layout Note:
Place these resistors
close to the CRT-out
connector

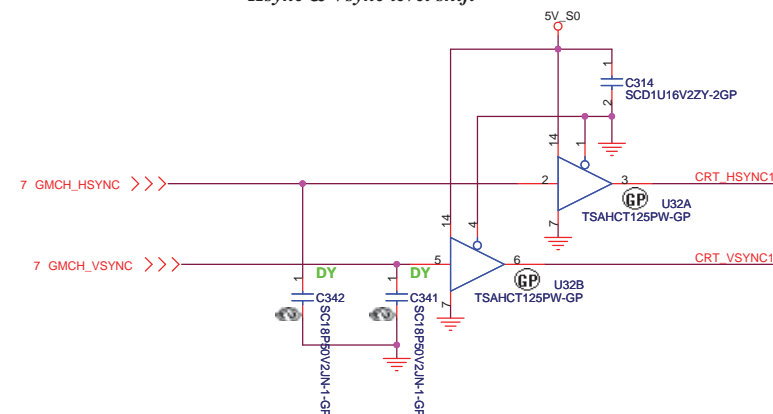
Ferrite bead impedance: 10 ohm@100MHz



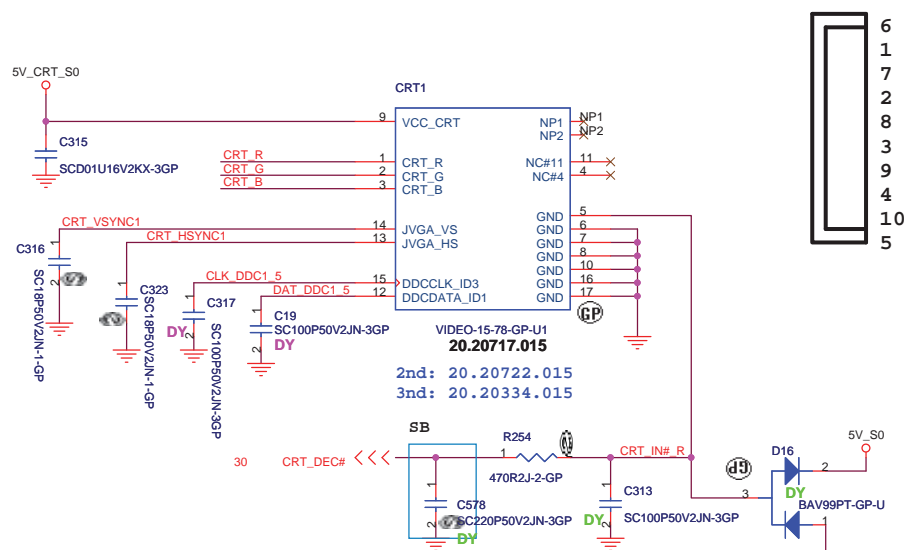
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

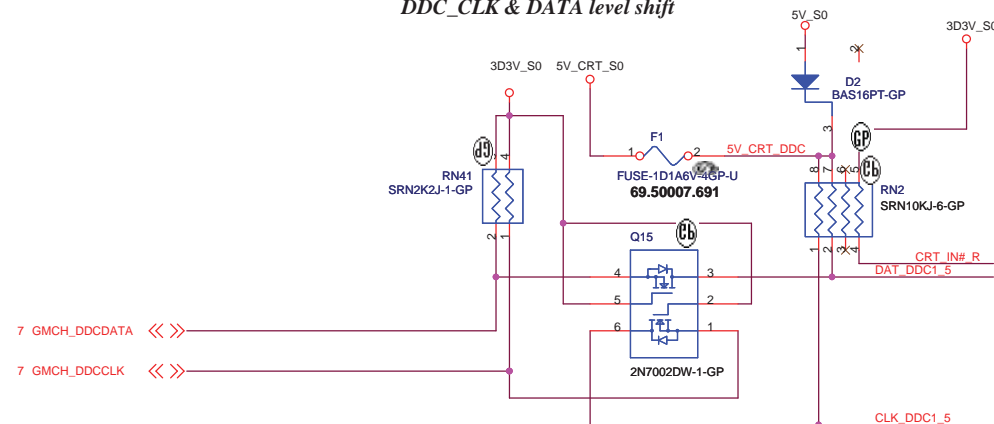
Hsync & Vsync level shift



CRT I/F & CONNECTOR



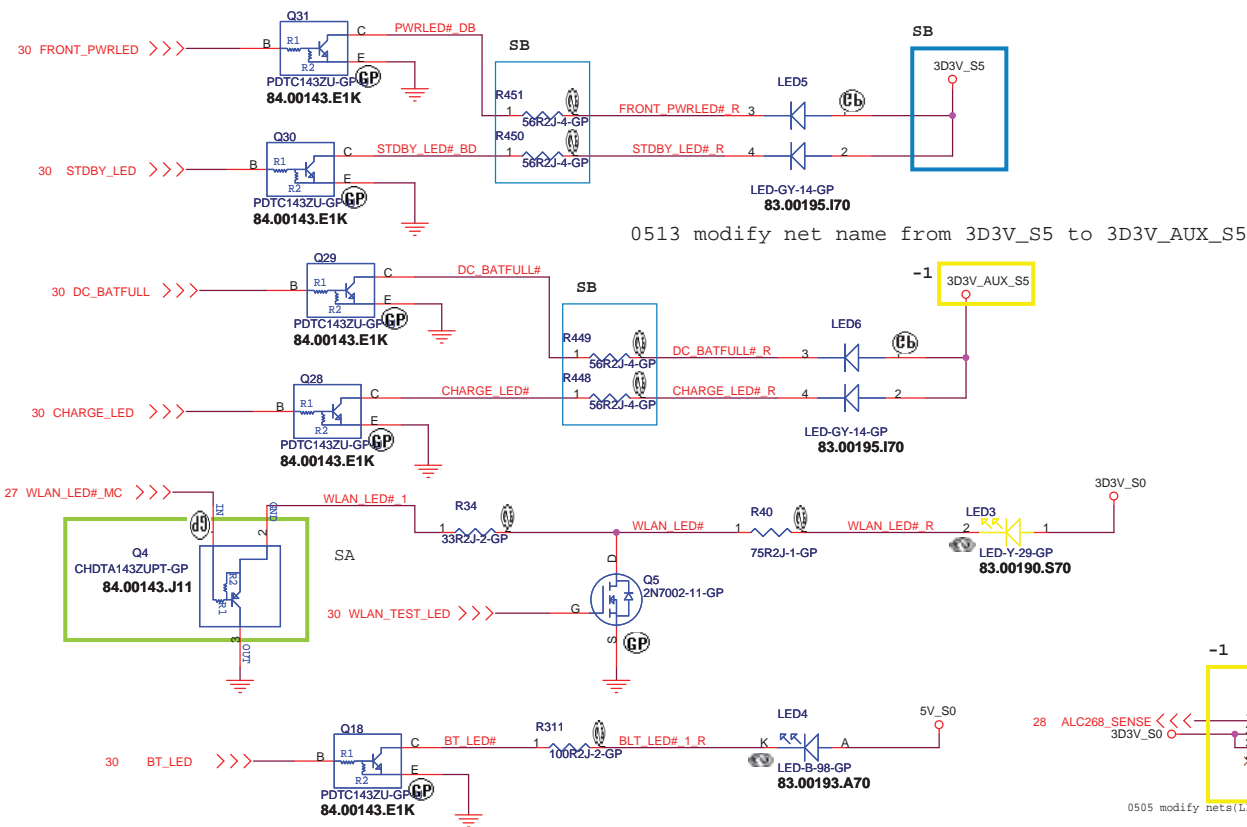
DDC_CLK & DATA level shift



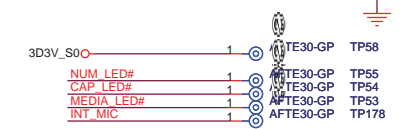
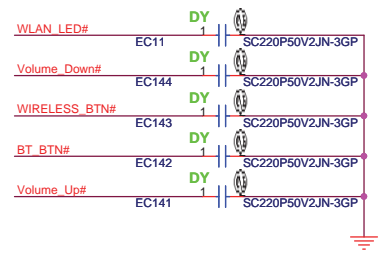
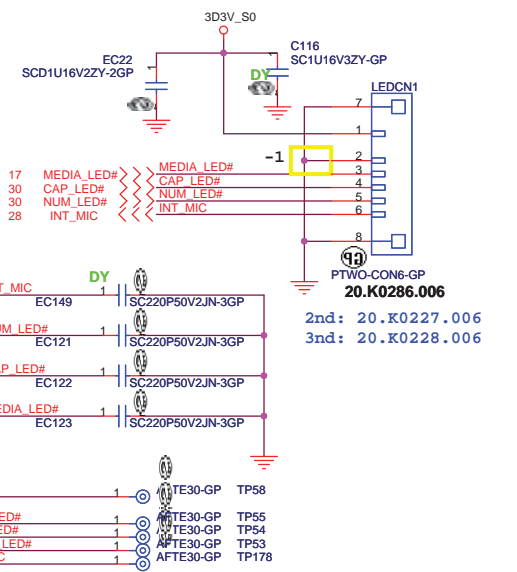
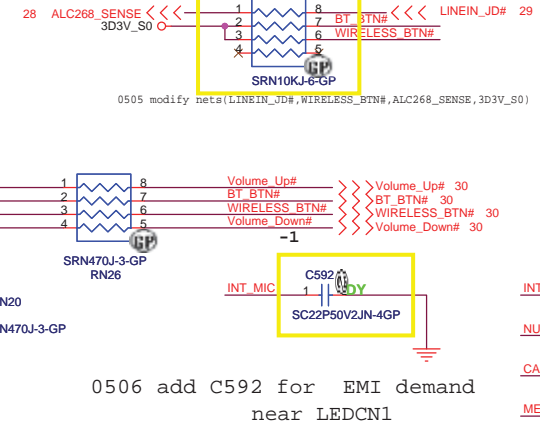
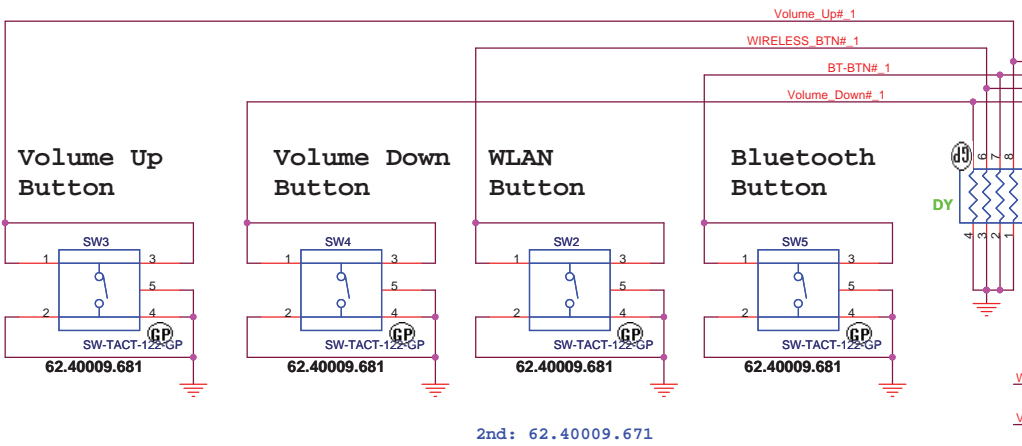
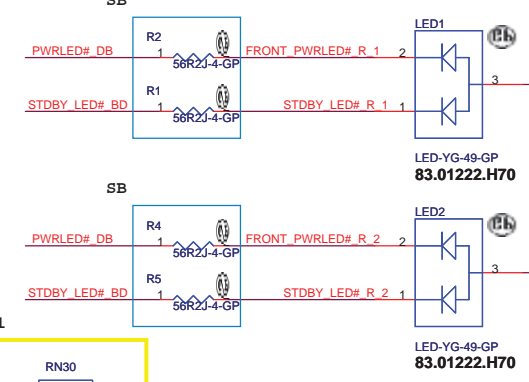
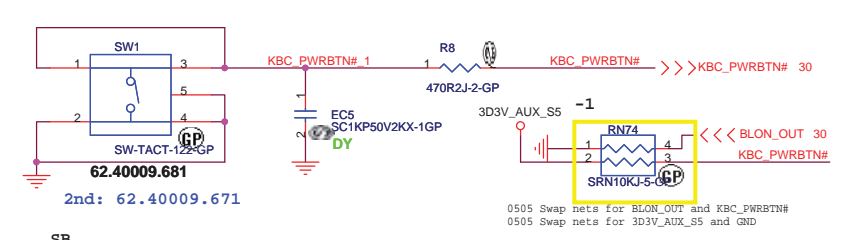
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Title			
CRT Connector			
Size	Document Number		Rev
	Cathedral Peak		-
Date: Thursday, May 15, 2008		Sheet 15 of	42

<http://hobi-elektronika.net>



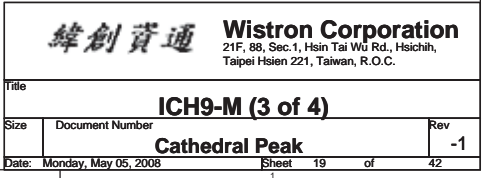
Power Button

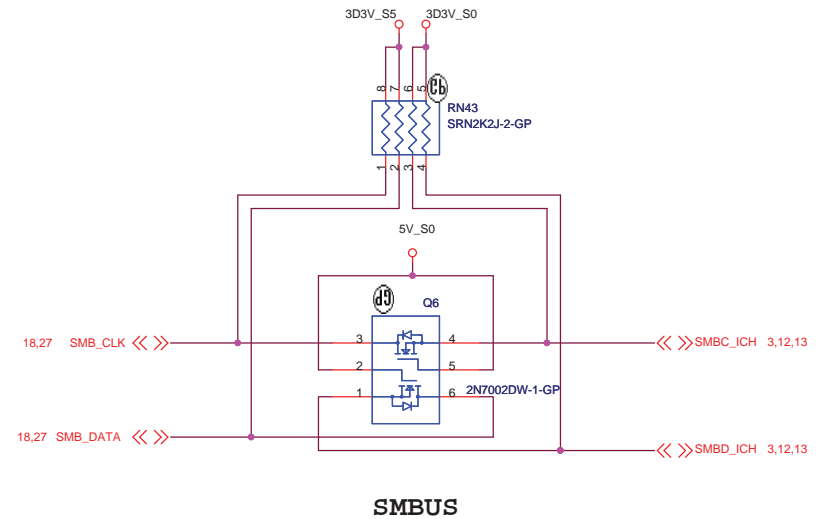
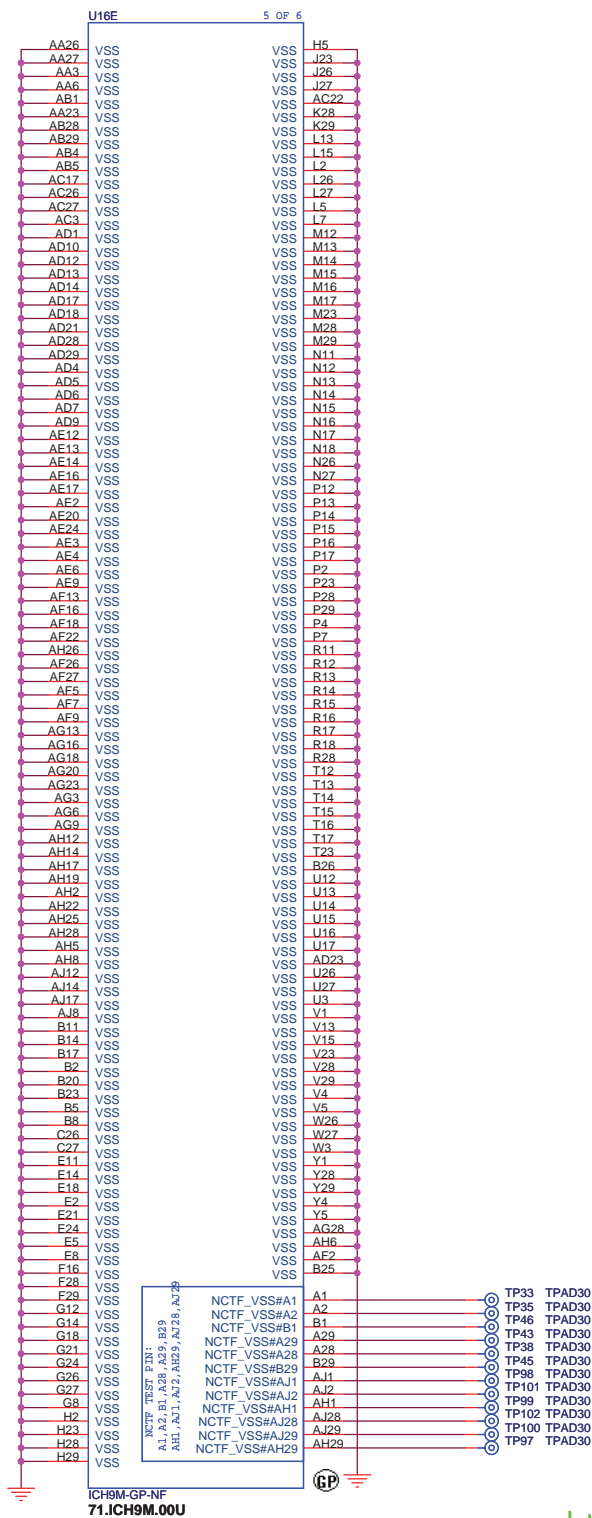


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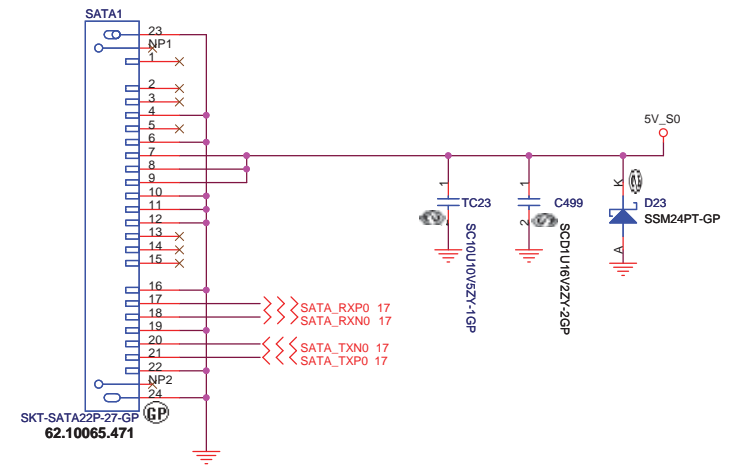
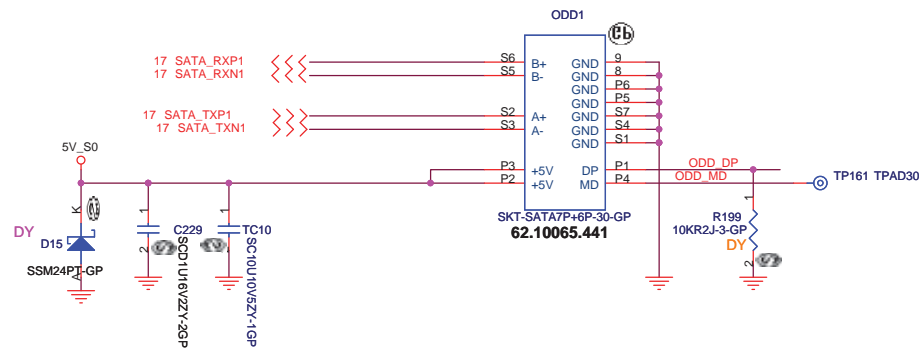
POWER /LAUNCH/LED BOARD		
Size	Document Number	Rev
		-1
Date: Friday, May 16, 2008	Sheet 16 of 42	

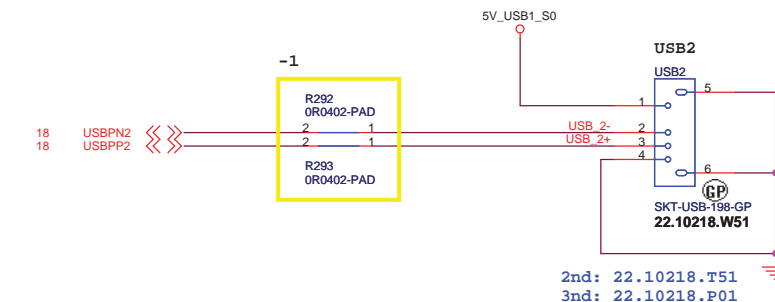
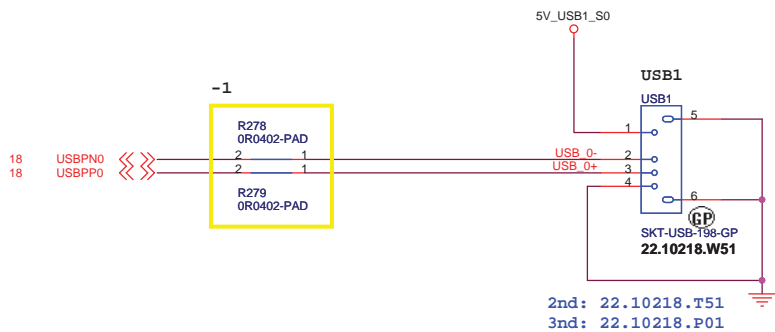






SATA Connector

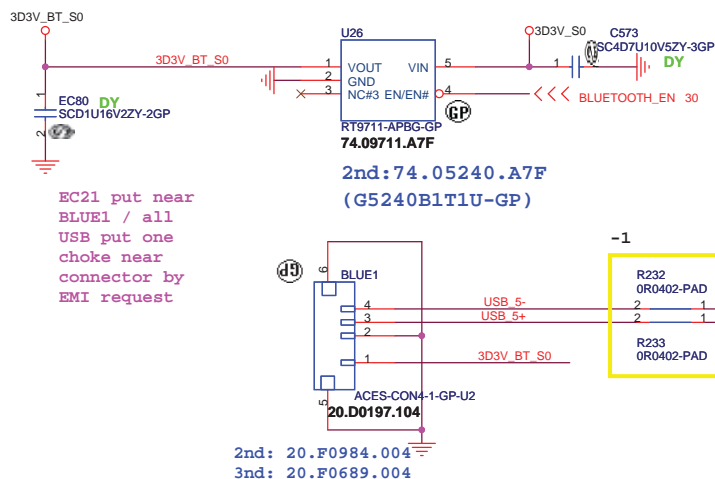




Co-Layout Common Mode Choke and 0 Ohm

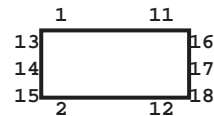
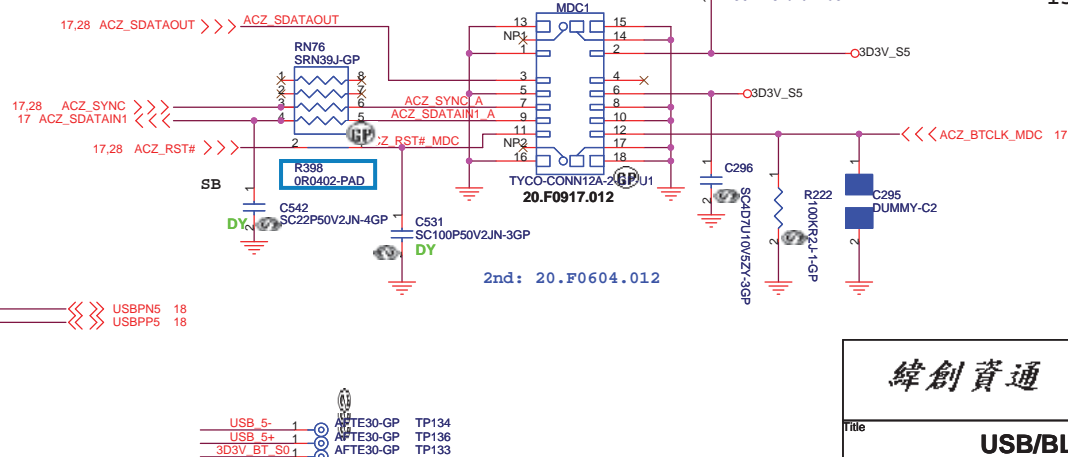
BLUETOOTH MODULE

1.5A / High Active Voltage 2V

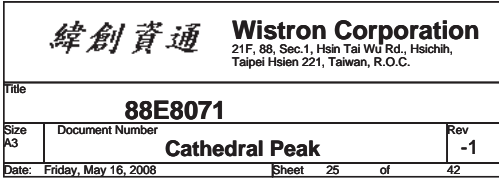


EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

MDC 1.5 CONN



<http://hobi-elektronika.net>

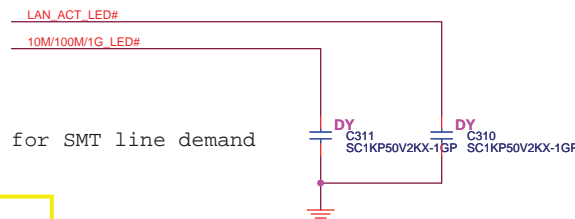
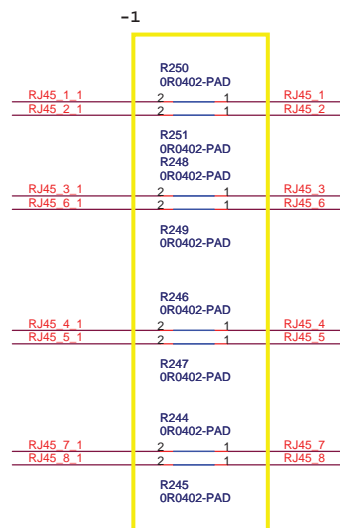
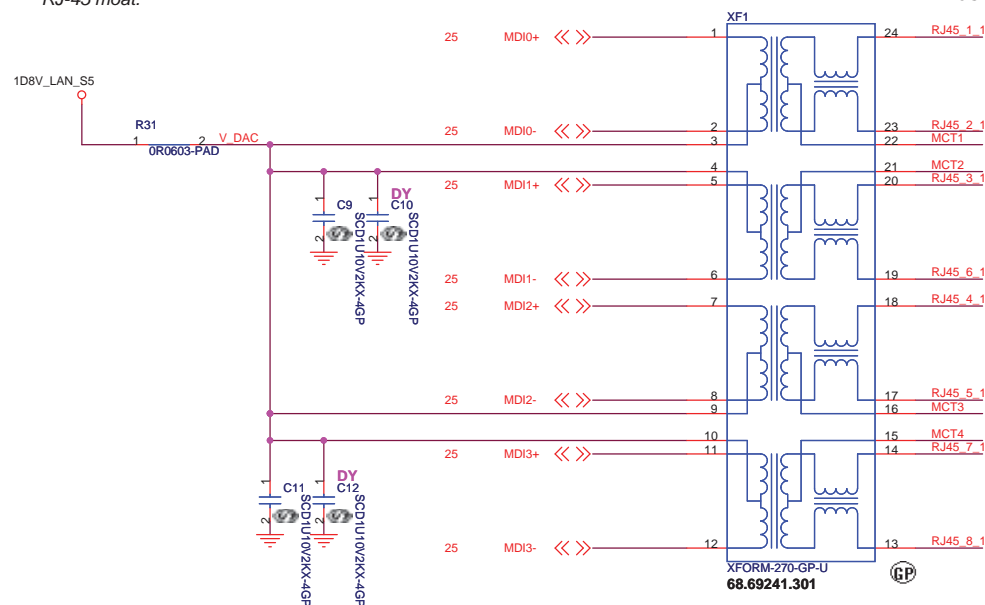


LAN Connector

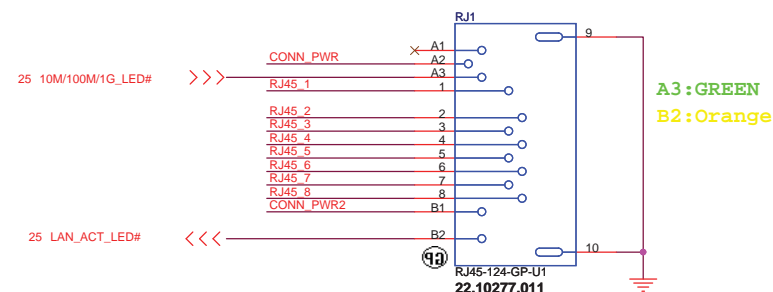
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

Co-Layout Common Mode Choke and 0 Ohm

0507 delete RN36~RN39 for SMT line demand



LAN Connector

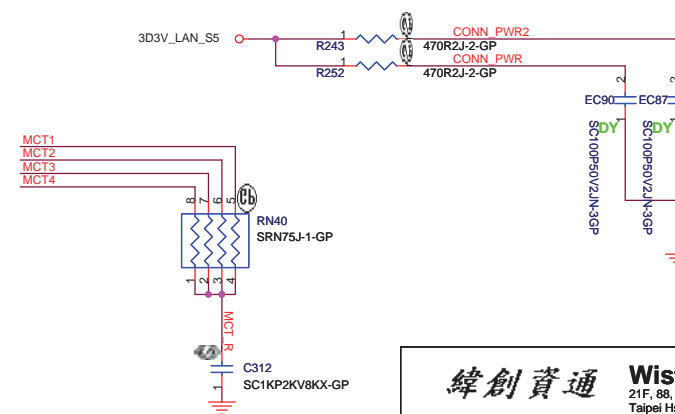


2nd: 22.10277.061

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

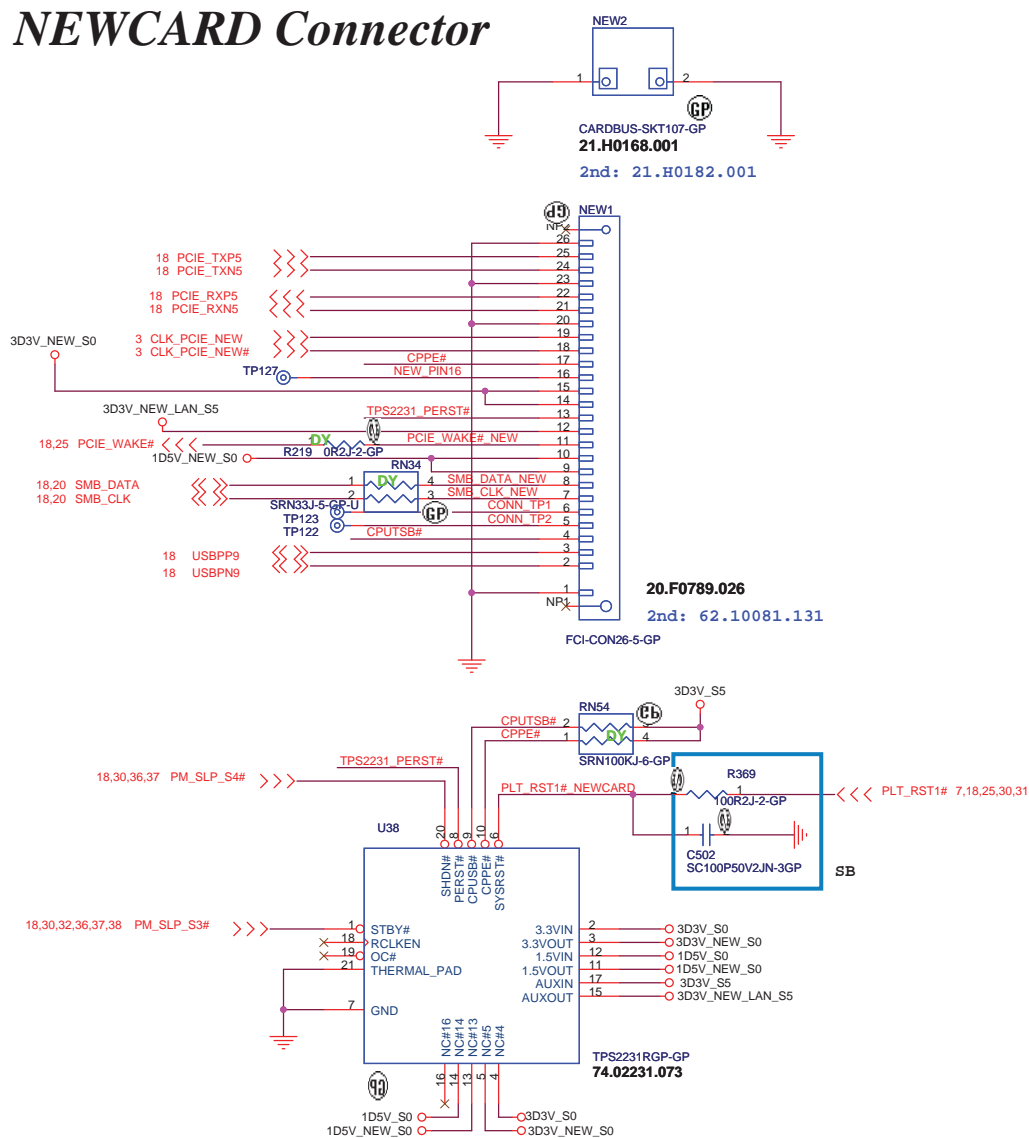
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



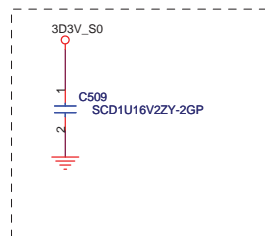
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
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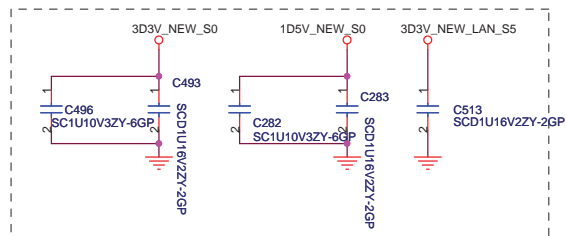
NEWCARD Connector



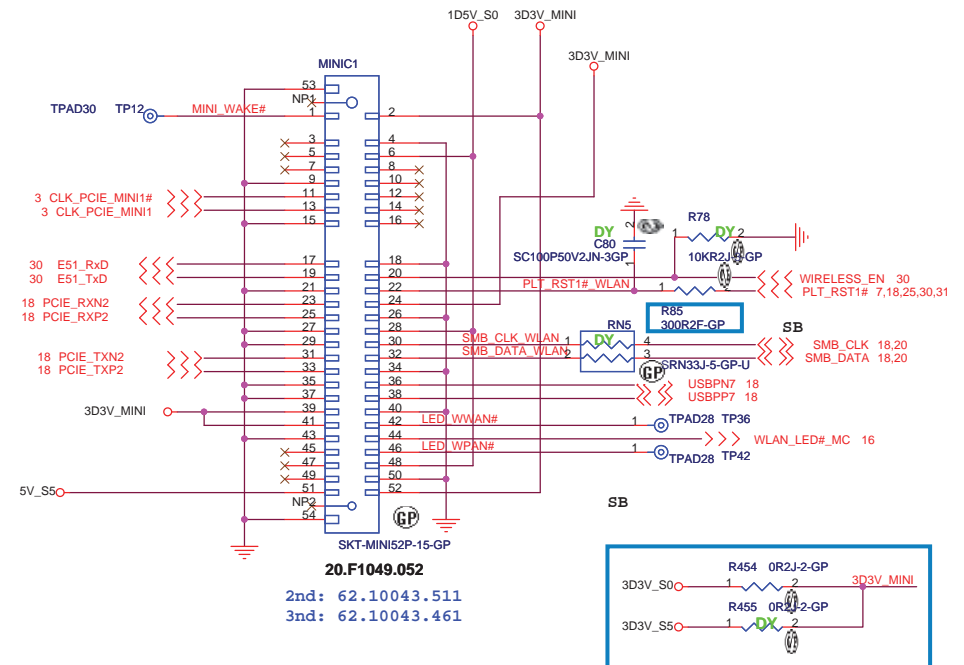
Place them Near to Chip



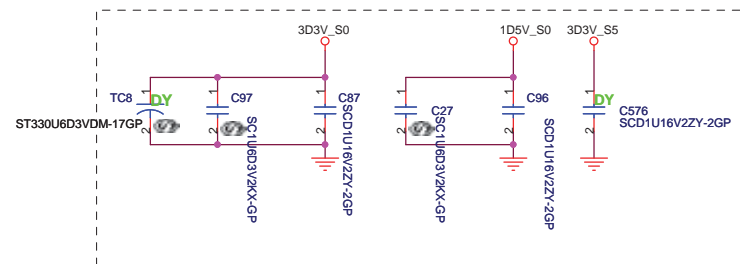
Place them Near to Connector

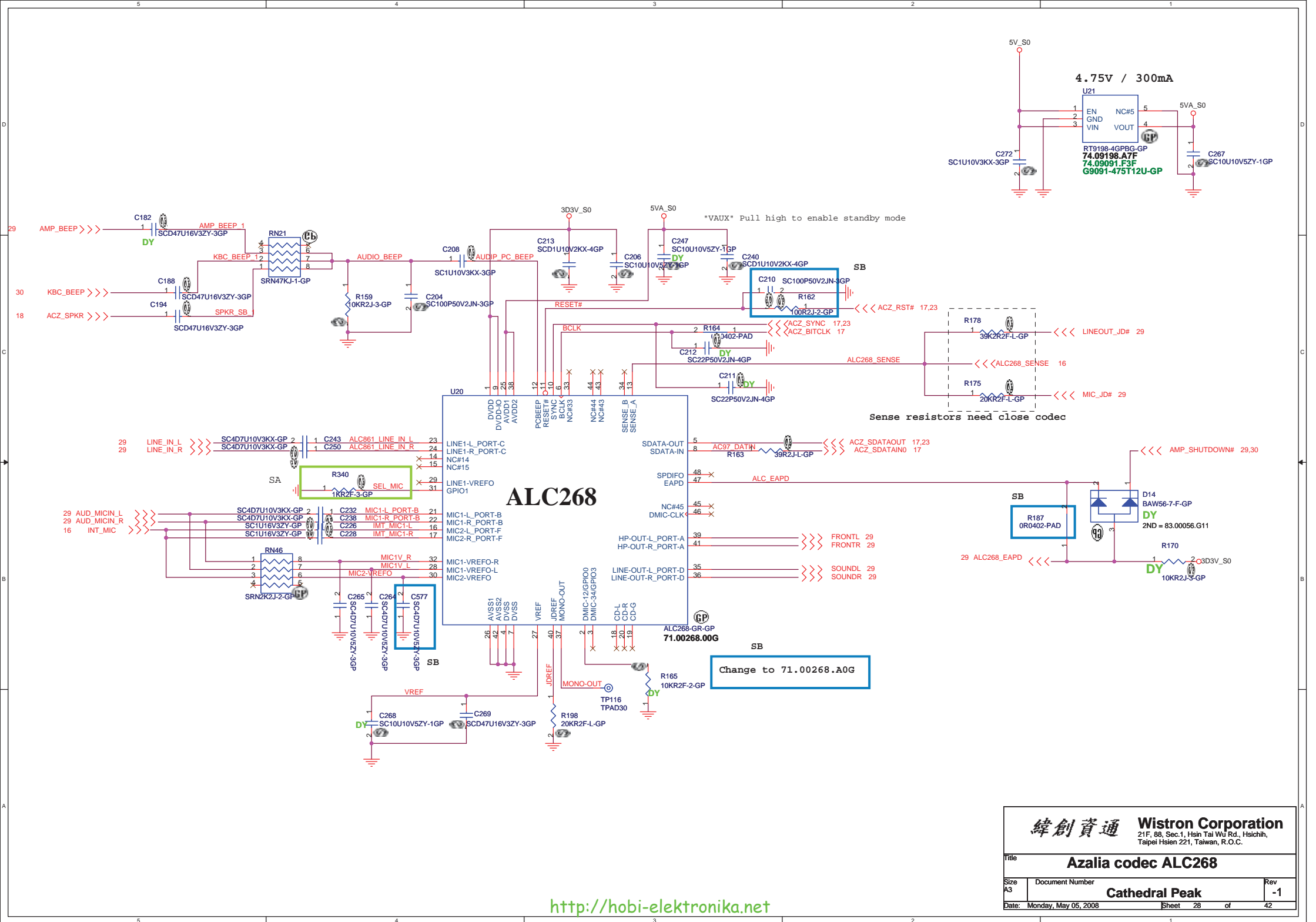


Mini Card Connector(WLAN)

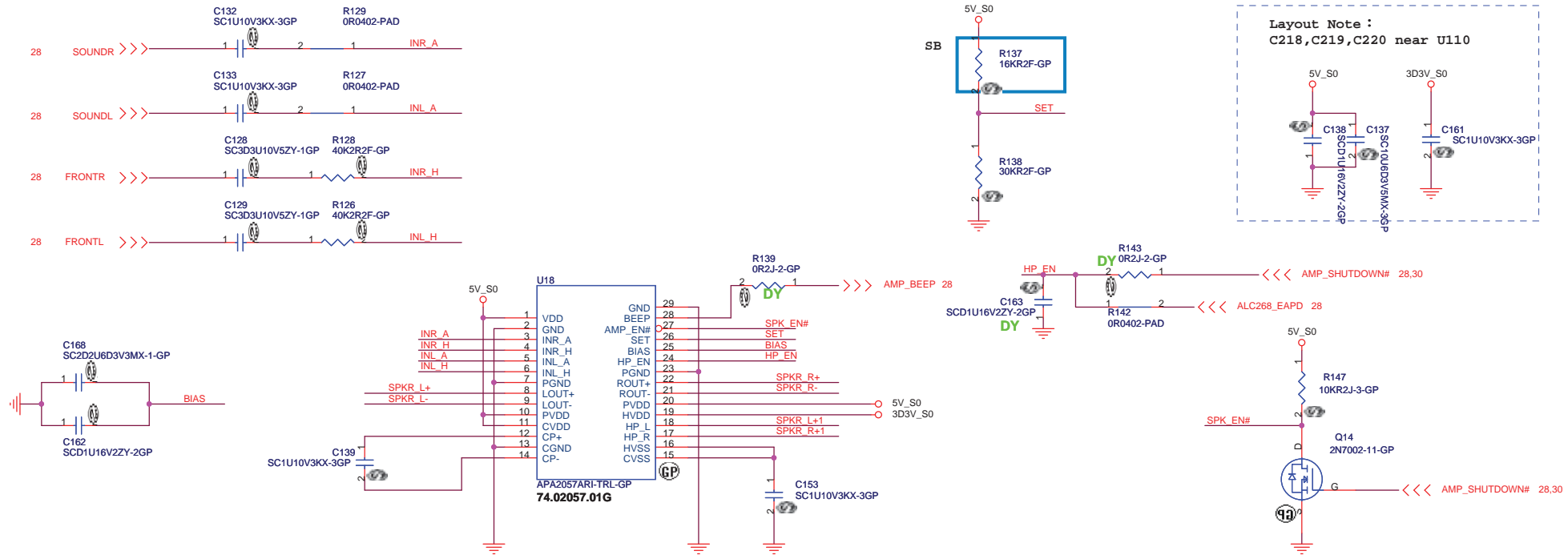


Place near MINIC1

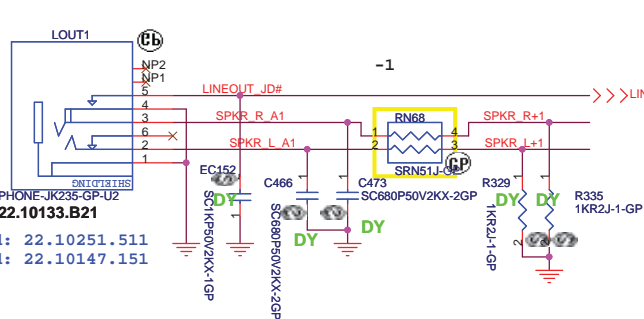




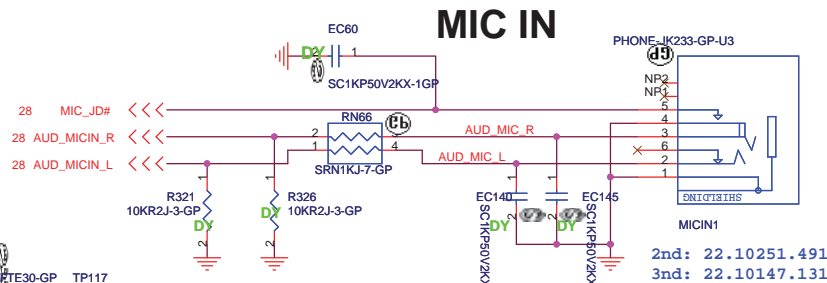
AUDIO OP AMPLIFIER



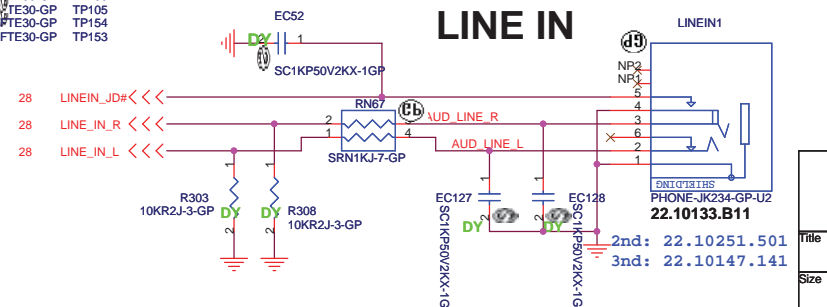
LINE OUT



MIC IN

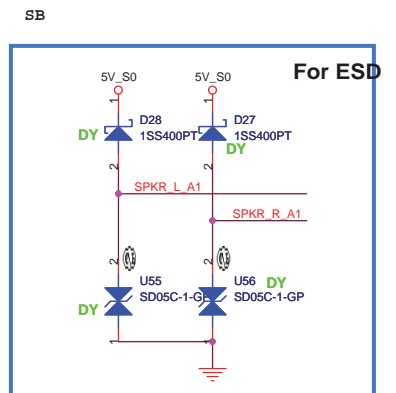


LINE IN



Analog Int. Mic

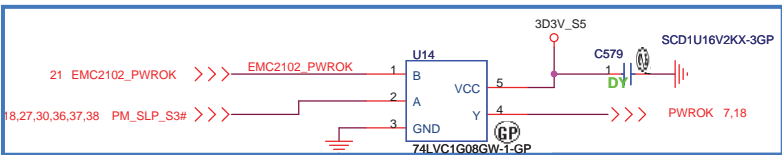
remove to LED Board

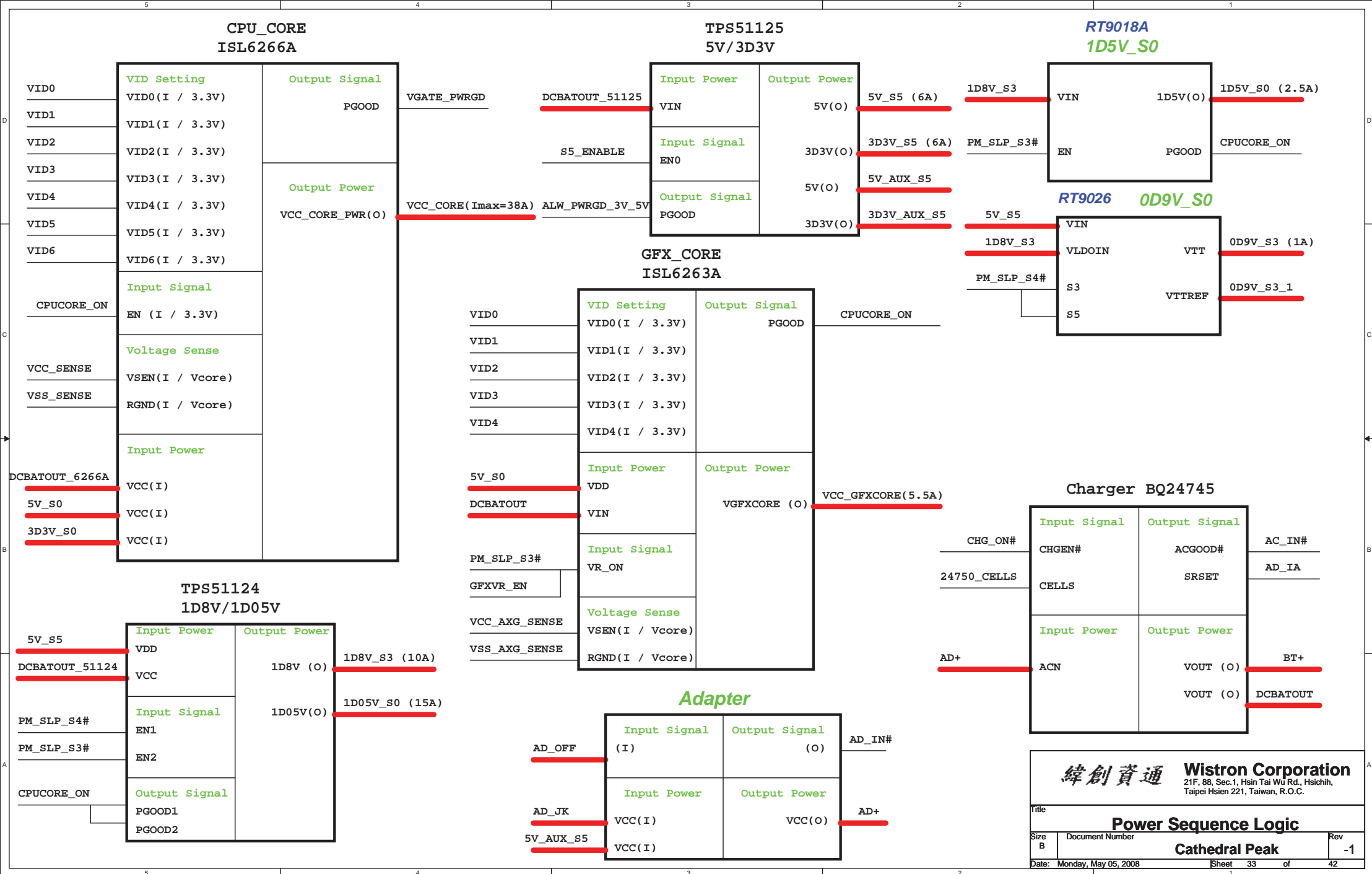


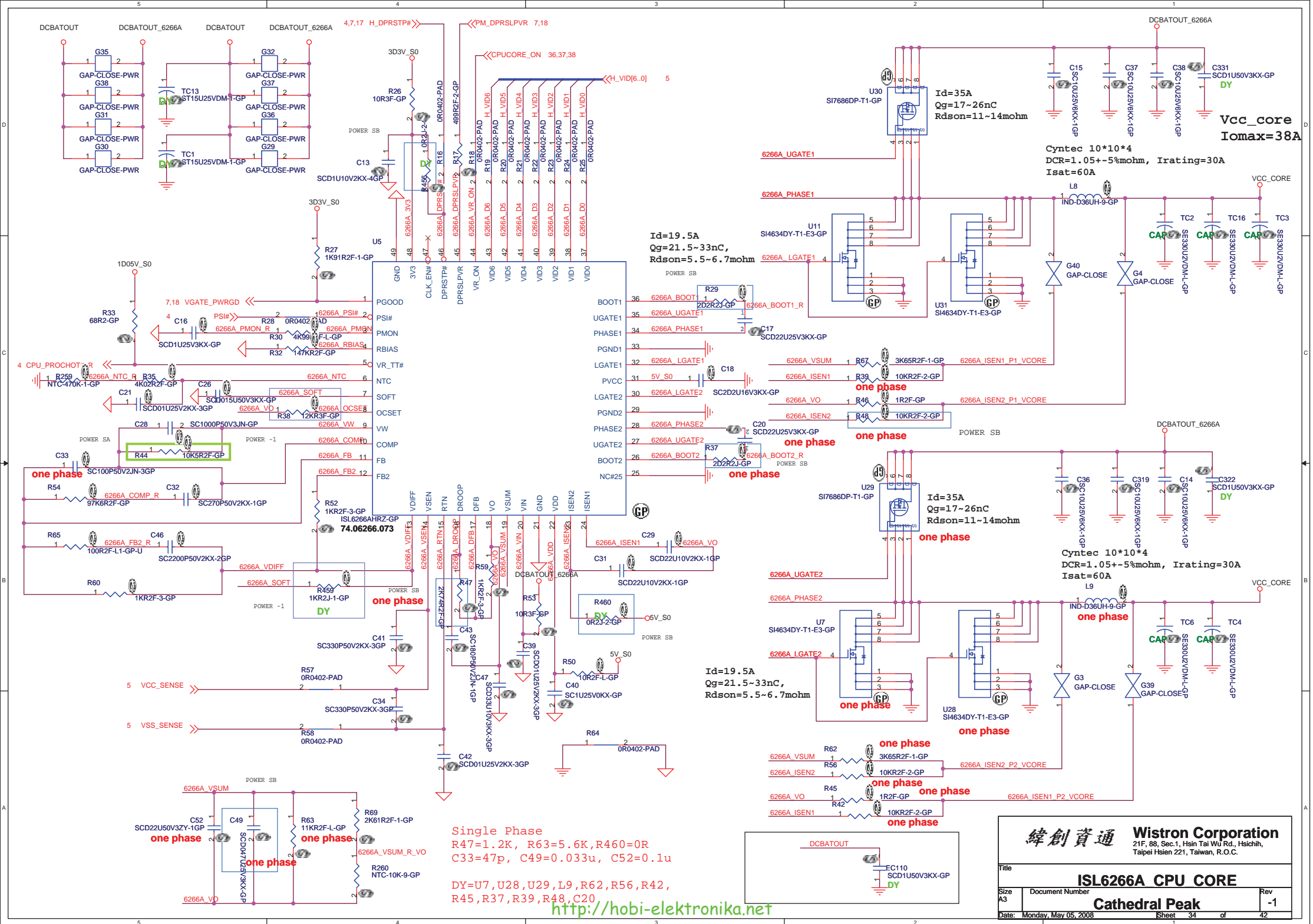
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AUDIO AMP AND JACK			Rev
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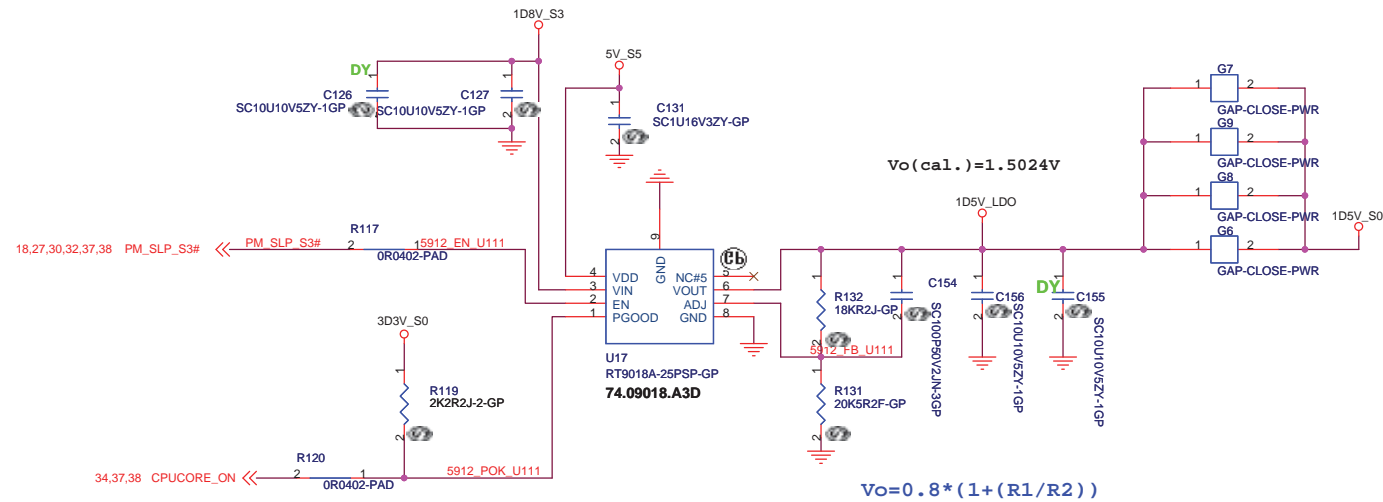
Run Power



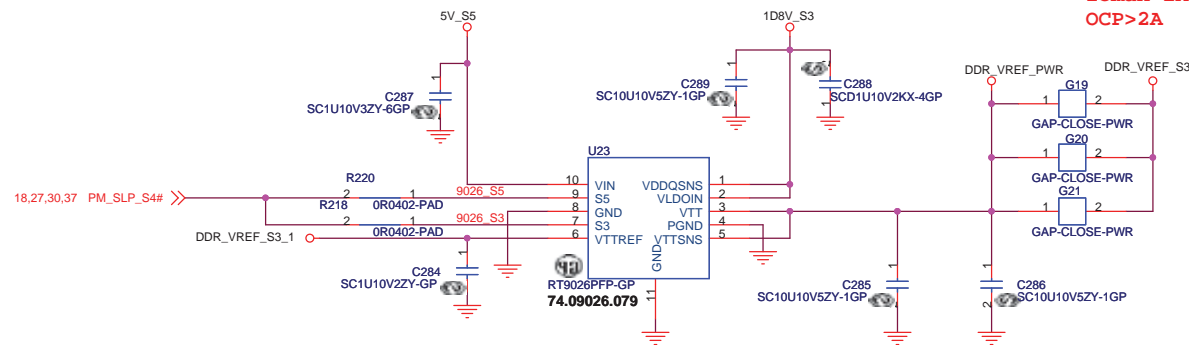




1D5V_S0
Iomax=2.5A

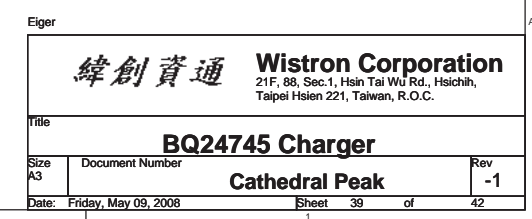


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OCP>2A

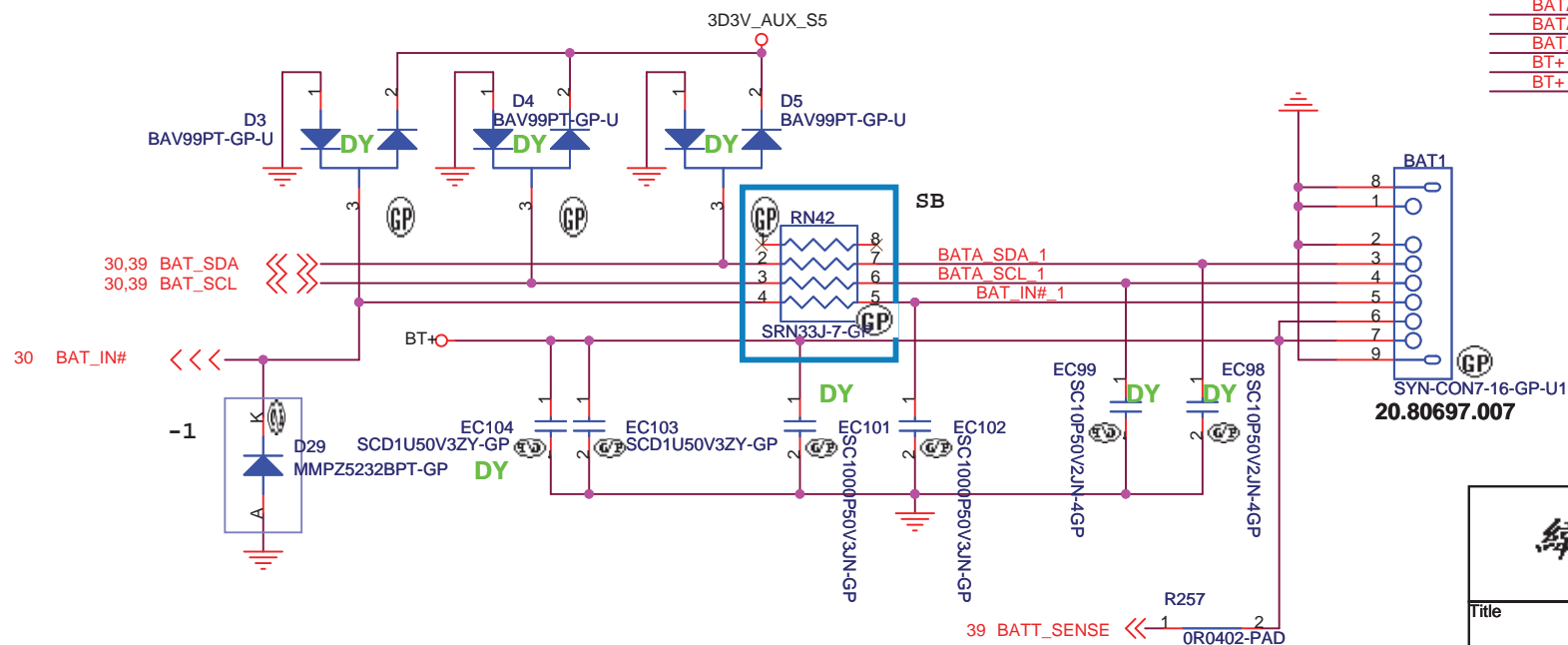


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1D5V & 0D9V		
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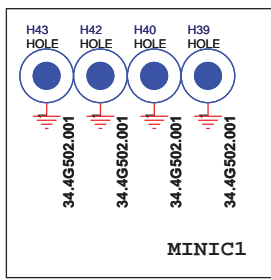
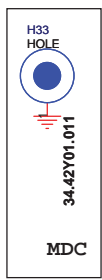
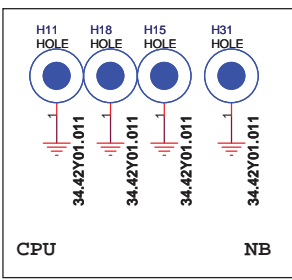
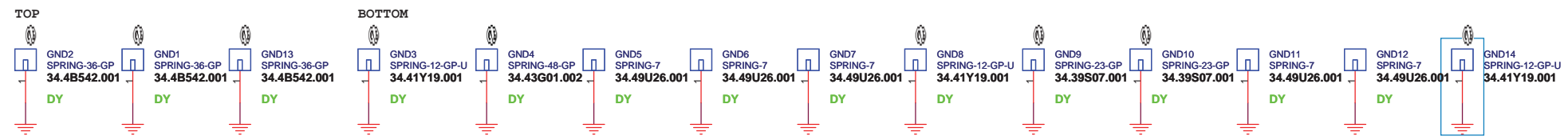
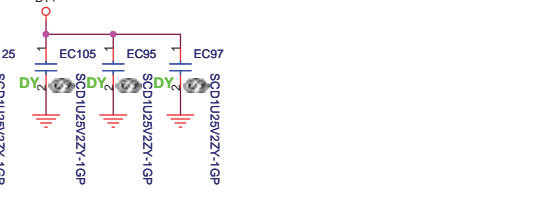
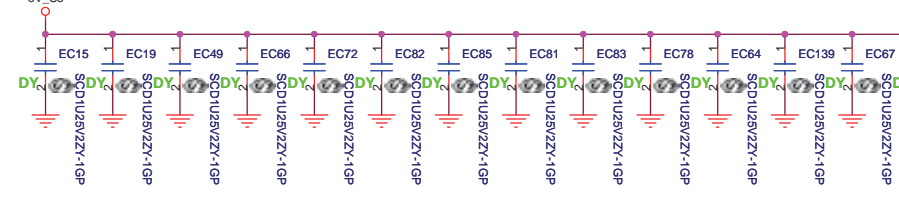
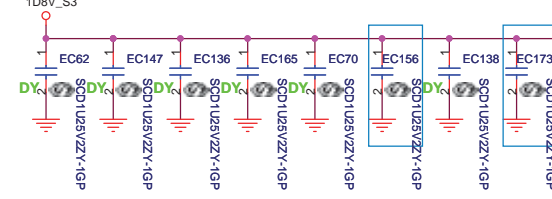
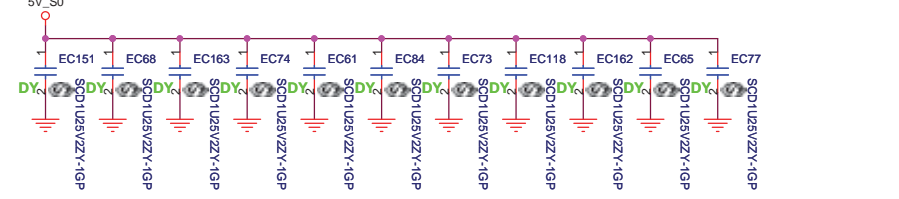
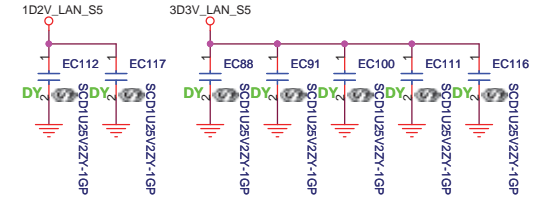
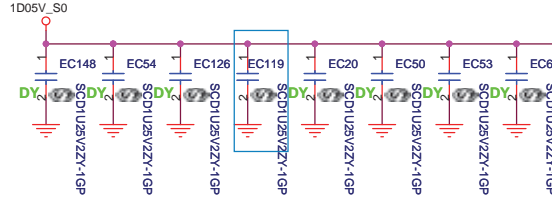
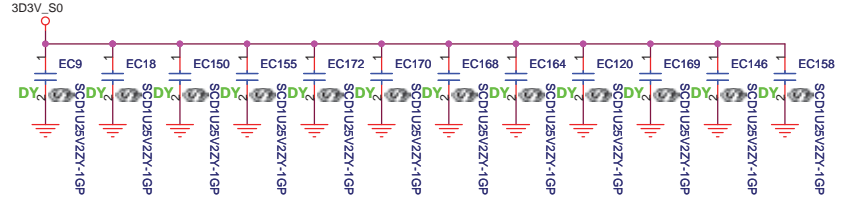
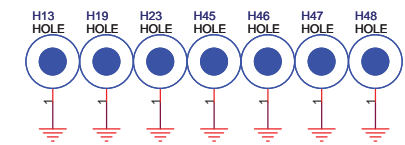
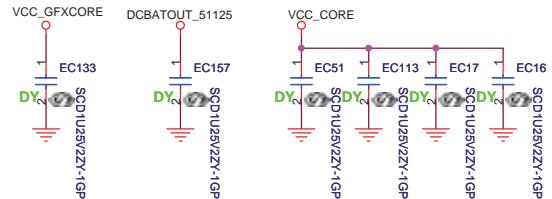
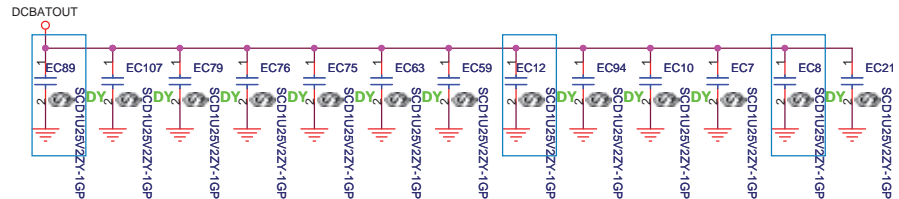
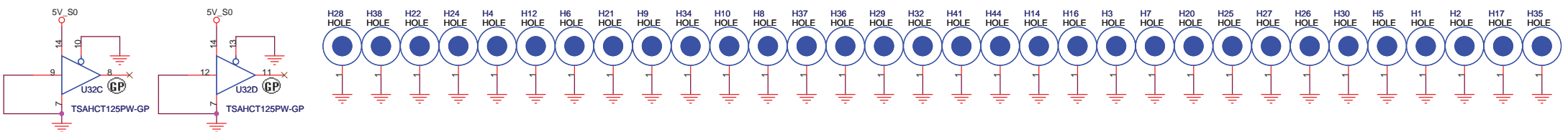


BATTERY CONNECTOR



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Check test point



0505 modify TP179~TP186

Test Point放在Dimm Door打開可量測處

http://hobi-elektronika.net


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SB to -1
1.charge_LED issue
Pgae16--->Modify net name from 3D3V_S5 to 3V_AUX_S5
2.delete common mode coke
Pgae26--->delete RN36-RN39
3.modify test point size
Pgae41--->modify TP179~TP186
4.delete common mode coke
Pgae23--->delete RN35,RN44,RN48
5.Page30-->add R461
6.Page35-->Reserve TC27 for Power team
7.Page38-->modify these values of R227,C551,C552 forPower team
8.Page40-->modify the part of D29
9.Page29-->modify the value of RN68
EMI
1.Page14--->Reserve C590,C591
2.Page16--->Reserve C592
3.Page17--->Reserve C593,C594
4.Page24--->Reserve C581~C589 and add R462

Merge
1.R309,RN9(4P2R) change to RN9(8P4R)
2.R172,RN30(4P2R) change to RN30(8P4R)
3.R152 change to RN59
4.R143,R151change to RN70
5.R213,R211 change to RN71
6.R200,R201,R202 change to RN72
7.R9,R240 change to RN74
8.R272,R81change to RN75
9.R402,R402 change to RN76
10.RN57(4P2R),RN69(4P2R) change to RN57(8P4R)
11.ER1,ER3,RE4 change to ERN1
12.
13.
14.
15.

0 Ohm change to PAD
R427,R117,R120,R218,R220

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Title			
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